CFP2/CFP2-ACO Kit Interconnects' Manual

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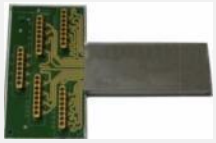
MSA Compliant CFP2 4x25G Gb/s Passive Host

ML4027

MSA Compliant CFP2 4x25G Gb/s Retimed Loopback Module

ML4029

10 x 10 GB/s CFP2 Breakout Module



ML4028

MSA Compliant CFP2 10x10G Gb/s Passive Host

ML4042

MSA Compliant CFP2 10x10G Gb/s Passive Loopback Module

ML4030

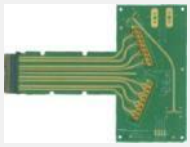
MSA Compliant CFP2 10x10G Gb/s Retimed Loopback Module

ML4043

MSA Compliant CFP2-ACO 4x25G Gb/s Passive Host

ML4027-ACO

MSA Compliant CFP2-ACO 4x25G Gb/s Breakout Module



ML4028-ACO

MSA Compliant CFP2-ACO 4x25G Gb/s Passive Host

ML4030-ACO

User Manual for the CFP2 and CFP2-ACO 100 Gb/s Electrical Loopback Modules, CFP2 and CFP2-ACO Host & Breakout Module

User Manual Version 0.0.6
Sept 11th, 2014
Product Model Numbers: **ML4027, ML4027-ACO, ML4028, ML4028-ACO, ML4029, ML4030, ML4030-ACO, ML4042, ML4043**

MultiLane S.A.L., Houmal Technology Park, Houmal.

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1. General Safety Summary

CAUTION. This warning symbol means danger. You are in a situation that could cause bodily injury or could result in damage to this product or other property. Before you work on any equipment, be aware of the hazards involved with electrical circuitry and be familiar with standard practices for preventing accidents.

2. Required Tools

You need these tools to install the CFP2 transceiver modules:

• Wrist strap or other personal grounding device to prevent ESD occurrences.

3. Glossary of Terms/ Acronyms

MSA: Multi Source Agreement.
NVR: Non Volatile Registers.
NVM: Non Volatile Memory.

4. Preface

This is the user manual of the CFP2 Electrical Loopback Modules along with the CFP2 Passive Host Module. It covers the following information:

- The MultiLane CFP MSA values as they are organized in the “CFP MSA Management Interface Specification” data sheet REV1.4.
- Describes the capabilities of the instrument: how to manage its operation.

4.1 About This Manual

This manual is composed of the following sections:

- Getting started introduces you an overview, the features, capabilities, benefits, applications and the reference documents used in the development of this product.
- Recommended Operating Conditions, led indications, a summary and the MSA Memory MAP.

5. Products Description

5.1 Overview

Our **CFP2 Electrical Loopback** is packaged in a standard MSA housing compatible with all CFP2 ports. Used for testing CFP2 transceiver ports, and provides an easy method of servers and blades testing instead of using optical modules. Transmitted data through the host is electrically routed, (internal to the loopback module or through Retimer chip), to the receive data inputs and back to the host.

- It provides an economical way to exercise CFP2 ports during R&D validation, production testing, and field testing.
- The **ML4029** provides 4 lanes at 25Gb/s, in retimed loopback mode.
- The **ML4043** provides 10 lanes at 10Gb/s, in retimed loopback mode.
- The **ML4030** provides 10 lanes at 10Gb/s, in passive loopback mode.

Our **100G CFP2 Compliant Host** test boards **ML4027** and **ML4042** are designed to provide an efficient and easy method of programming and testing CFP2 modules.

- The **ML4027/ML4042** comes complete with operations software and user manual to enable intuitive testing. As well as designed to simulate an ideal environment for CFP2 module testing. These properties make the host board as electrically transparent as possible, allowing a more accurate assessment of the modules' performance.

The **ML4029**, **ML4043** and **ML4030** can be used alone along with the customer Host tool, or with our **ML4027/ML4042** CFP2 Hosts to ensure a complete test solution is provided.

6. CFP2 Loopback Modules User Guide Manual

6.1 ML4029- CFP-2 4x25G Retimed Loopback Module Key Features

- 4 TX & 4 RX Lanes, high-speed signals.
- High performance Signal Integrity traces.
- MSA compliant Digital Diagnostic and Monitoring Interface (DDMI).
- 3 Status LED indicator.
- Built with advanced Rogers™ material.
- Retimed Loop back mode at all 25G Rates.
- PRBS Generator & Detector supports all pattern lengths
- Loss of Signal Detection.
- Programmable output level for receiver sensitivity.
- Temperature sensing.
- Hot Pluggable module.

6.1.1 Benefits

- Economical CFP2 Port Testing
- Custom Memory Maps
- Board Level System Testing
- Retimed Loopback Mode
- BER Capability

6.1.2 LED Indicator

Green (Solid) - Signifies that the module is operating in high power permitted mode as defined by the CFP MSA specification.

Amber (Solid) - Signifies the module is operating in low power mode as defined by the CFP MSA specification.

Green/Amber (Blinking) - Signifies that the module is overheated and the temperature high alarm is asserted.

6.1.3 Applications

- *At Speed Dynamic line card testing.*

6.1.4 Operation Conditions

Parameter	Symbol	Notes/Conditions	Min	Typ	Max	Units
Operating Temperature	T_A		0		75	°C
+3.3V Supply Voltage	VCC	Main Supply Voltage		3.3		V
Data Rate	R_b	Guaranteed to work at 10Gbps per lane, achieving a total rate of 100Gbps		100		Gbps
Power Class				1		

Table 1 Recommended Operation Conditions

6.2 ML4030-CFP-2 10x10G Passive Loopback Module Key Features

-10 TX & 10 RX Lanes, high-speed signals.

- High performance Signal Integrity traces.
- MSA compliant Digital Diagnostic and Monitoring Interface (DDMI).
- 3 Status LED indicator.
- Built with advanced Rogers™ material.
- Temperature sensing.
- Programmable Power Dissipation from 3W to 12 W.
- Hot Pluggable module.
- Cut-off temperature automatically switches the module to low power state to avoid overheating.

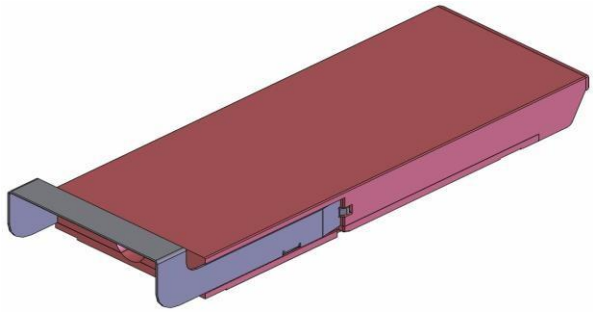


Figure 1: CFP2 Loop Back

6.2.1 Benefits

- Economical CFP2 Port Testing
- Custom Memory Maps
- Board Level System Testing
- Emulates all CFP2 Power classes

6.2.2 LED Indicator

Green (Solid) - Signifies that the module is operating in high power permitted mode as defined by the CFP MSA specification.

Amber (Solid) - Signifies the module is operating in low power mode as defined by the CFP MSA specification.

Green/Amber (Blinking) - Signifies that the module is overheated and the temperature high alarm is asserted.

6.2.3 Applications

- *CFP2 Port Compliance Testing*

6.2.4 Operation Conditions

Parameter	Symbol	Notes/Conditions	Min	Typ	Max	Units
Operating Temperature	T_A		0		75	°C
+3.3V Supply Voltage	VCC	Main Supply Voltage		3.3		V
Data Rate	R_b	Guaranteed to work at 10Gbps per lane, achieving a total rate of 100Gbps		100		Gbps
Power Class Emulates all power classes					3W to 12W	W

Table 2 Recommended Operation Conditions

6.3 ML4043-CFP-2 10x10G Retimed Loopback Module Key Features

-10 TX & 10 RX Lanes, high-speed signals

- High performance Signal Integrity traces

- MSA compliant Digital Diagnostic and Monitoring Interface (DDMI)

- 3 Status LED indicator

- Built with advanced Rogers™ material

- Retimed Loop back mode at all 10G Rates

- Equalizes deteriorated input signals

- provides electrical compensation to cable, copper, and backplane environments to increase system margin and media driving distances

- Input & DFE Adaptation to Optimize Eye opening

- Loss of Signal Detection

- Wide Range CRU

- Programmable output level for receiver sensitivity

- PRBS Checker

- Temperature sensing

- Hot Pluggable module

6.3.1 Benefits

- Economical CFP2 Port Testing
- Custom Memory Maps
- Board Level System Testing
- Retimed Loopback Mode

6.3.2 LED Indicator

Green (Solid) - Signifies that the module is operating in high power permitted mode as defined by the CFP MSA specification.

Amber (Solid) - Signifies the module is operating in low power mode as defined by the CFP MSA specification.

Green/Amber (Blinking) - Signifies that the module is overheated and the temperature high alarm is asserted.

6.3.3 Applications

- *At Speed Dynamic line card testing.*

6.3.4 Operation Conditions

Parameter	Symbol	Notes/Conditions	Min	Typ	Max	Units
Operating Temperature	T_A		0		75	°C
+3.3V Supply Voltage	VCC	Main Supply Voltage		3.3		V
Data Rate	R_b	Guaranteed to work at 10Gbps per lane, achieving a total rate of 100Gbps		100		Gbps
Power Class				1		

Table 3 Recommended Operation Conditions

6.4 Plugging the CFP2 Loopback module into the Host

CAUTION. The CFP2 transceiver module is a static-sensitive device. Always use an ESD wrist strap or similar individual grounding device when handling CFP2 transceiver modules or coming into contact with system modules.

To install a CFP2 transceiver module, follow these steps:

1. Attach an ESD wrist strap to yourself on one end and a properly grounded point on the chassis or the rack on the other end.
2. The CFP2 transceiver module is located inside its metallic shell.
3. Hold the shell so that the identifier label is on the top.
4. Align the CFP2 shell in front of the Host module's transceiver socket opening.
5. Carefully slide the CFP2 shell into the socket until the transceiver makes contact with the socket electrical connector.

6.5 General Description

6.5.1 Overview of CFP management Interface

It is the main communication interface between a Host and a CFP2 module. Host uses the interface to control and monitor the start up, shutdown, and normal operation of the module. This interface operates over a set of hardware pins through the CFP2 module connector and software based protocols (the primary protocol is specified using MDIO bus structure).

The CFP2 loop back device has the following circuit diagram:

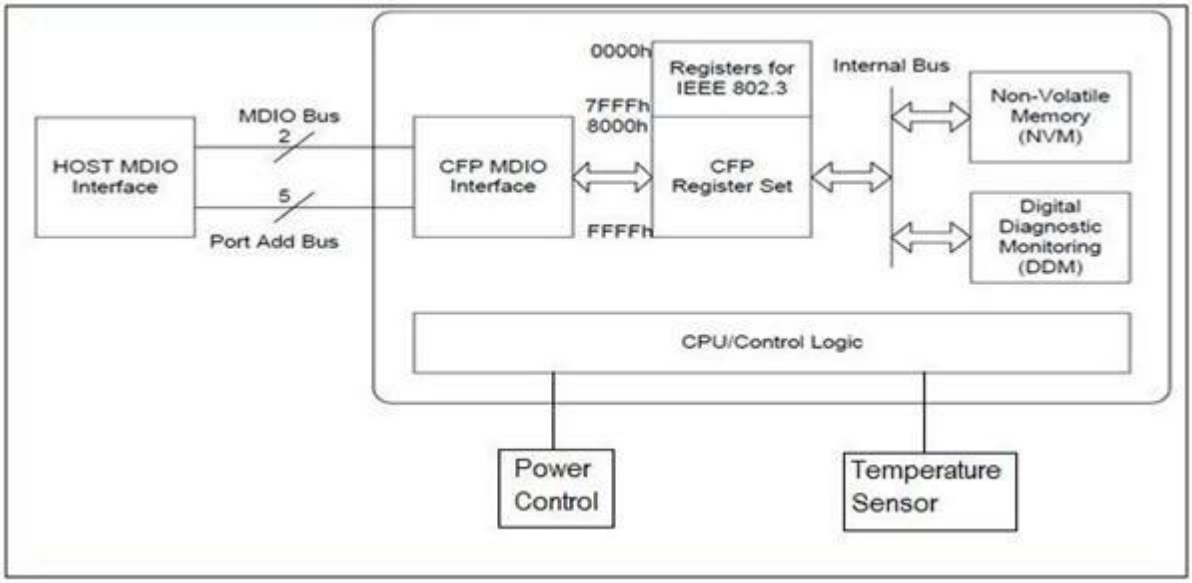


Figure 2: CFP2 Loop Back Block Diagram

From a hardware point of view, CFP Management Interface consists of 8 hardware signals: 2 hardware signals of MDC and MDIO, 5 hardware signals of Port Address PRTADR0-4, and 1 hardware signal GLB_ALRMn. MDC is the MDIO Clock line driven by the Host and MDIO is the bi-directional data line driven by both the Host and module depending upon the data directions.

From a software/protocol point of view, CFP Management Interface consists of the MDIO management frame, a set of CFP registers, and a set of rules for host control, module initialization, and signal exchange between these two.

6.5.2 High Speed Signals

The Electrical High Speed Bus Basically Transfers the TX inputs of the module to the RX outputs, and is either connected in passive loopback mode as in ML4030, or looped back through a retimer chip as in ML4029 and ML4043.

10x10 Modules (ML4030 and ML4043) have a High Speed Bus operating at 10Gb/s.

4x25 Module (ML4029) is capable of operating at speed up to 28Gb/s, Typically the High Speed Bus operates at 25Gb/s.

6.6 Interface Architecture

A dedicated MDIO logic block in the CFP2 module to handle the high rate MDIO data and a CFP register set that is divided into two register groups, the Non-Volatile Registers (NVR) and the Volatile Registers (VR). The NVRs are connected to a Non-Volatile Memory device for ID/Configuration data storage. Over the internal bus system, the VRs are connected to a device that executes the Host control commands and reports various Digital Diagnostic Monitoring (DDM) data. Note in the rest of this documentation, independent of implementation, CFP registers are also referred as NVRs or VRs.

Our CFP2 module **ML4029,ML4030,ML4043** specifications are the following:

a) Supports of MDC rate up to 4MHz.

b) CFP Registers at MDIO Device Address 1 as specified by CFP MSA.

c) Supports various Physical Addresses thus allowing to communicate with many modules plugged in the same Host.

CFP registers use fast memory to shadow the NVM data and the DDM data. The shadow registers decouple the Host-side timing requirements from the module's internal processing, timing, and hardware control circuit introduced latency.

CFP shadow register set meets the following requirements:

a) It supports dual access from the Host and from module internal operations such as NVM and DDM data transfers.

b) It supports continuous Host access (read and write) with fast access memory at maximum MDC rate of 4 MHz.

c) It allows the uploading of NVM content into the CFP register shadow during module initialization. The data saving from CFP register shadow to NVM is supported.

d) It supports the DDM data update periodically during the whole operation of the module. The maximum data refresh period is 1ms (real time temperature monitoring).

e) It supports the whole CFP register set including all NVRs and VRs.

f) Incomplete or otherwise corrupted MDIO bus transactions are purged from memory and disregarded.

g) The port address is allowed to change in fly without a module reset.

7. CFP2 Loopback Modules Functional Description

7.1 CFP2 Common Specifications (for ML4029, ML4030 and ML4043)

The Functionalities listed below are common to all Multilane CFP2 loopback modules.

They are implemented and can be used in each of the modules : ML4029, ML4030 and ML4043

7.1.1 CFP Initialization sequence

This is the Startup sequence for the CFP2 modules:

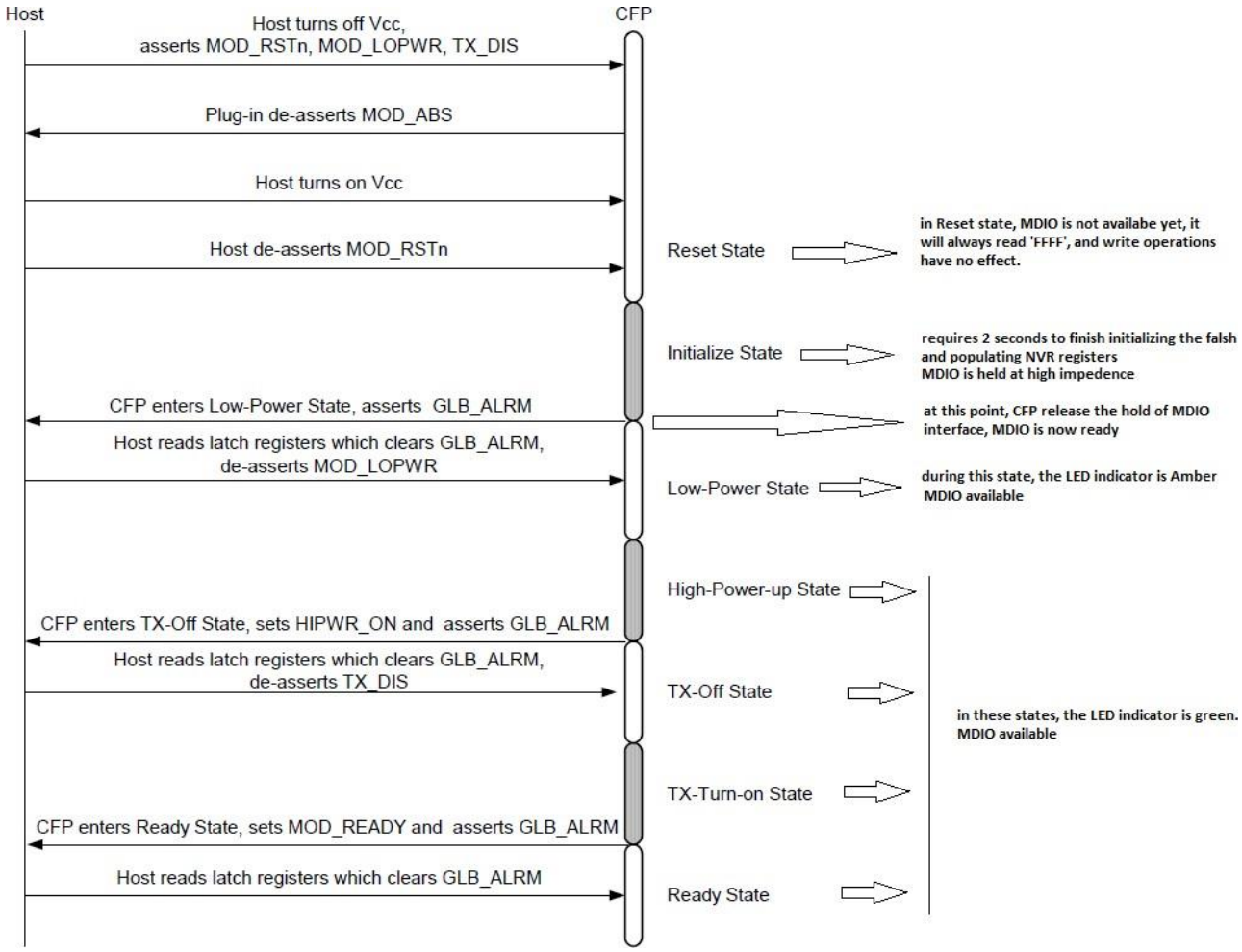


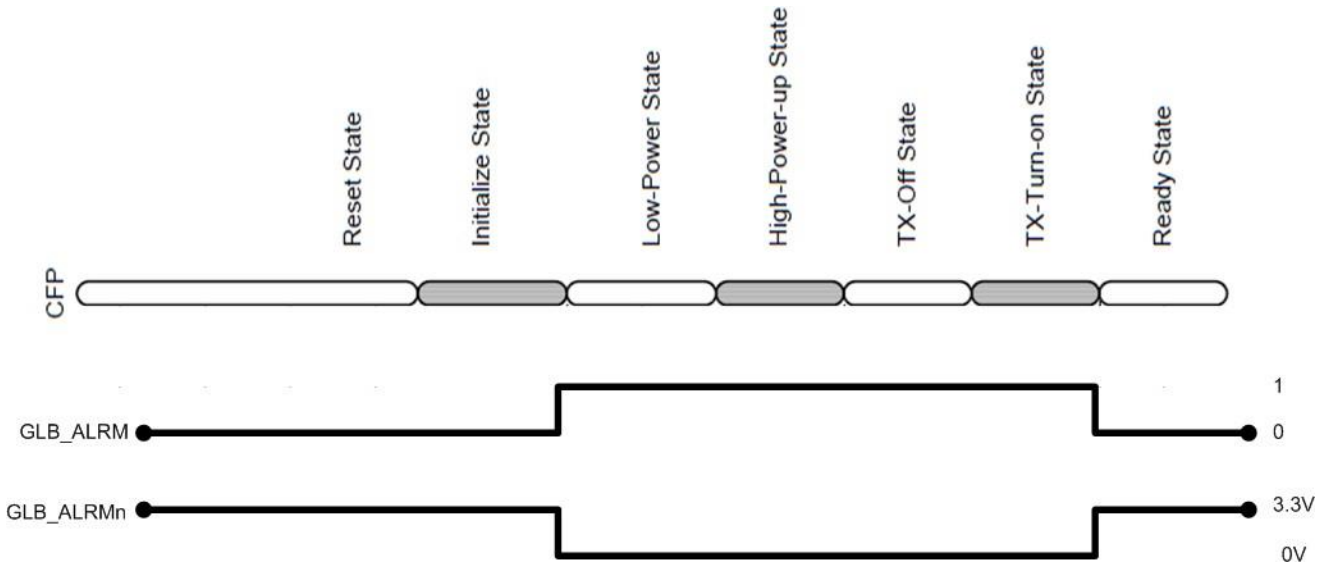
Figure 3 CFP Initialization sequence

MOD_RSTs assertion causes CFP2 module to reset, at this stage MDIO interface will be held at high impedance state, the Host will read 'FFFF'h, from any address, while host write operations will have no effect. Upon the de-assertion of MOD_RSTs, CFP2 module exists to initialize state which is a transient state.

The Initialization time required is 2 seconds. When Initialization state is done, CFP2 module will enter Low-Power state, at this point MDIO becomes available for R/W operations.

GLB_ALRM

Below is the flowchart for GLB_ALRM signal during CFP states transitions :



GLB _ALRM is de-asserted during Reset and Initialize state, it is asserted in Low-Power,High-Power-up, Tx-Off and TX-Turn-on states, then de-asserted again when ready state is reached. GLB_ALRMn is the hardware pin, and is the inverse of GLB_ALRM.

7.1.2 MDIO SIGNALS, addressing and frame structure

As per the port address used, the module will work on any MDIO Physical port address which can be set by the HW input signals PRTADR[2:0]. So when using 2 or more CFP2 slots, each of them can be configured to a different Port Address.

PRTADR0	MDIO Physical Port address bit 0
PRTADR1	MDIO Physical Port address bit 1
PRTADR2	MDIO Physical Port address bit 2

Table 4 MDIO Physical Port Address

The MDIO Device Address consists of 5 bits that are sent in MDIO frames, CFP MSA specifies that CFP register Set should be addressed using Device Address = 1.

The Below Frame shows all segments of an MDIO Packet, PHYADR are the 5 bits Physical Address and DEVADD are the 5 bits Device Address.

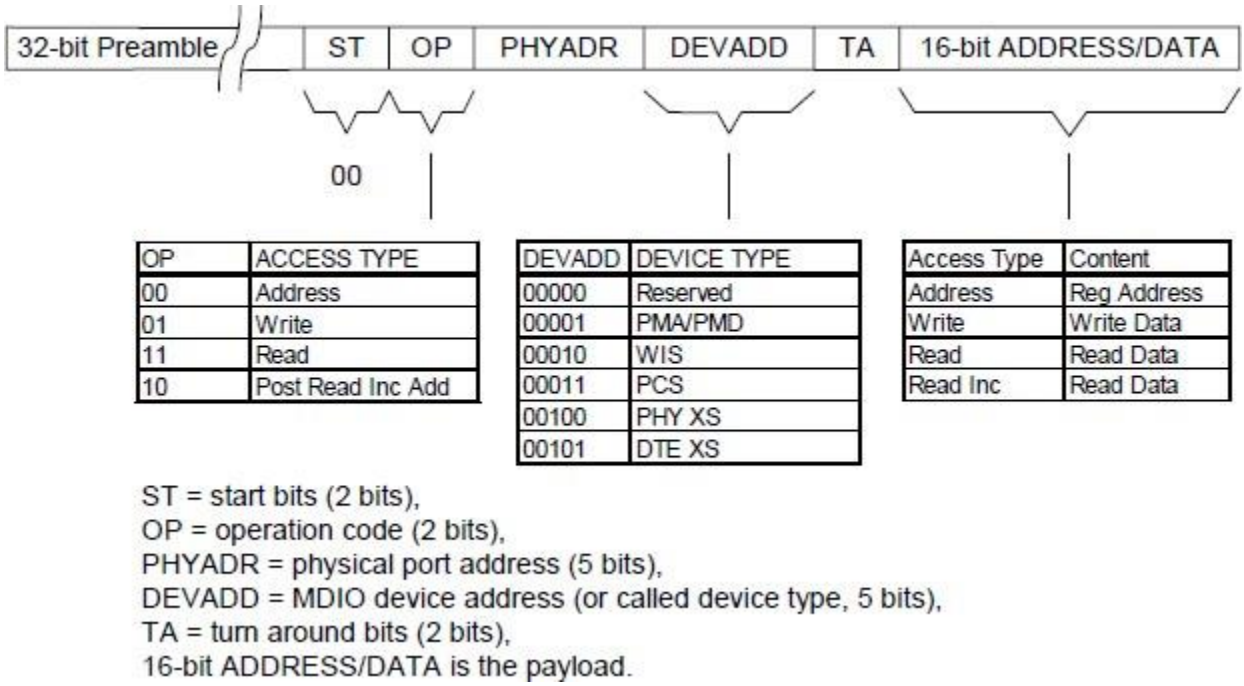


Figure 4 CFP MDIO Management Frame Structure

7.1.3 CFP Register Set

All registers from 0x8000 to 0x A47F are supported in memory map (Refer to table below), the set of registers starting from **0x8000 to 0x9F00** are implemented as **NVR registers**, all these registers are always read from NVM during initialization and mapped to corresponding address.

All **VR (Volatile Registers)** from **0xA000 to 0xA47F** are set to zero upon module power up.

The NVR values are saved to NVM by calling the SAVE NVR function. The base ID registers are initially set, but user can change as desired.

CFP Register Allocation					
Starting Address in Hex	Ending Address in Hex	Access Type	Allocated Size	Data Bit Width	Table Name and Description
8000	807F	RO	128	8	CFP NVR 1. Basic ID registers.
8080	80FF	RO	128	8	CFP NVR 2. Extended ID registers.
8100	817F	RO	128	8	CFP NVR 3. Network lane specific registers.
8180	81FF	RO	128	8	CFP NVR 4.
8200	83FF	RO	4x128	N/A	MSA Reserved.
8400	847F	RO	128	8	Vendor NVR 1. Vendor data registers.
8480	84FF	RO	128	8	Vendor NVR 2. Vendor data registers.
8500	87FF	RO	6x128	N/A	Reserved by CFP MSA.
8800	887F	R/W	128	8	User NVR 1. User data registers.
8880	88FF	R/W	128	8	User NVR 2. User data registers.
8900	8EFF	RO	12x128	N/A	Reserved by CFP MSA.
8F00	8FFF	N/A	2x128	N/A	Reserved for User private use.
9000	9FFF	RO	4096	N/A	Reserved for vendor private use.
A000	A07F	R/W	128	16	CFP Module VR 1. CFP Module level control and DDM registers.
A080	A0FF	RO	128	16	Reserved by CFP MSA.
A100	A1FF	RO	2x128	N/A	Reserved by CFP MSA.
A200	A27F	R/W	128	16	Network Lane VR 1. Network lane specific registers.
A280	A2FF	R/W	128	16	Network Lane VR 2. Network lane specific registers.
A300	A3FF	RO	2x128	N/A	Reserved by CFP MSA.
A400	A47F	R/W	128	16	Host Lane VR 1. Host lane specific registers.

Table 5. CFP Register Set

7.1.4 User NVR Restore and Save Functions (0xA004)

To write permanently to User NVR registers (0x8000→ 0x9F00) Host shall use the "Save" function to store the shadowed data into underlying NVM. The host only needs to perform a single Save operation to copy the entire User NVR shadow registers to the underlying NVM after finishing editing the data.

Upon power-up or reset the User NVR shadow registers are "Restored" with NVM values. Note that the Restore function will overwrite the NVR shadow registers, losing any host-written values in them that have occurred since the last Save to the underlying NVM.

The NVR Access Control Register (**A004h**) provides the Save function for Host to save the User NVRs content.

Bit 5 in NVR Access Control Register is designated for User NVR save command.

A "1" written to bit 5 in register A004h initiates a User NVR Save.

So to call the user NVR save command user can write 0x0020 into register 0xA004.

The Save NVR duration is around 2 seconds. When this function is called it should be followed by a 2 second time wait.

During this process user can't write or read CFP registers.

7.1.5 PRG_ALRMs

The signals HIPWR_ON, MOD_READY, and MOD_FAULT are CFP internally generated signals and are defaults of the programmable alarm pins PRG_ALRMx.

The Following Table lists the corresponding functions for each of the PRG_ALRMs.

NAME	ALARM SOURCE	VALUE
HIPWR_ON	Module high-power-on indicator. PRG_ALRM1 MSA default.	0: Module not high powered up 1: Module high power up completed
MOD_READY	MOD_READY, module startup sequence done, PRG_ALRM2 MSA default.	0: Not done 1: Done
MOD_FAULT	Fault detected. PRG_ALRM3 MSA default.	0: No Fault 1: Fault

Table 6. Alarm Sources

7.1.6 Temperature Monitoring

The alarms and warnings of the CFP2 Loop Back are listed in the table 7, 8 and 9. Alarms and Warnings are set in register 0xA01F in bits 8,9,10 and 11, and are continuously asserted and de-asserted when the corresponding alarms/warnings occur. addresses 0x8080, 0x8082, 0x8084, and 0x8086 are reference registers for temperature alarms and warnings, they contain the default values (HA:75, HW:65, LW:5 and LA:0) and can be changed when desired. The module is continuously reading the temperature and storing its value in Register 0x A02F.

When The temperature reaches the High Alarm values, The module front LED indicator will begin blinking.

CFP NVR 2						
Hex Addr	*Size*	*Access Type*	*Bit*	*Register Name* *Bit Field Name*	*Description*	*LSB Unit*
Alarm/Warning Threshold Registers						
8080	2	RO	7~0	Transceiver Temp High Alarm Threshold	These thresholds are a signed 16-bit integer with LSB = 1/256 of a degree Celsius representing a range from -128 to + 127 255/256 degree C. MSA valid range is between –40 and +125C." MSB stored at low address, LSB stored at high address.	1/256 degC
8082	2	RO	7~0	Transceiver Temp High Warning Threshold		
8084	2	RO	7~0	Transceiver Temp Low Warning Threshold		
8086	2	RO	7~0	Transceiver Temp Low Alarm Threshold		

Table 7: Alarm / Warning Threshold Registers

CFP Module VR 1						
Hex Addr.	*Size*	*Access Type*	*Bit*	*Register Name* *Bit Field Name*	*Description*	*Init Value*
A01F	1	RO		Module Alarms and Warnings 1		0000h
			15~12	Reserved		0000b
			11	Mod Temp High Alarm	Mod temp high Alarm. (FAWS_TYPE_A) 0: Normal, 1: Asserted.	0
			10	Mod Temp High Warning	Mod temp high Warning. (FAWS_TYPE_A) 0: Normal, 1: Asserted.	0
			9	Mod Temp Low Warning	Mod temp low Warning. (FAWS_TYPE_A) 0: Normal, 1: Asserted.	0
			8	Mod Temp Low Alarm	Mod temp low Alarm. (FAWS_TYPE_A) 0: Normal, 1: Asserted.	0

Table 8: Module Temperature Alarms and Warnings

Module Analog A/D Value Registers						
A02F	1	RO	15~0	Module Temp Monitor A/D Value	Internally measured temperature in degrees Celsius, a 16-bit signed integer with LSB = 1/256 of a degree Celsius, representing a total range from -128 to + 127 255/256 degC. MSA valid range is between –40 and +125C. Accuracy shall be better than +/- 3 degC over the whole temperature range.	0000h

Table 9 Module Analog A/D Temperature Value Register

7.1.7 Insertion Counter

The Insertion counter contains the number of times the module was plugged in a host. The insertion counter is incremented every time the module goes in initializing sequence, as it is nonvolatile it is always saved, and can be read anytime from register 0x8400.

User can clear the insertion counter by writing 0 into 0x8400. The time constraint for this operation is between 1.5 and 1.7 seconds in order to erase the corresponding sector from the flash.

The registers for the insertion counter are as follow:

0x8400 : insertion_counter (LSB = 1 insertion) , representing a counter range from 0 to 255 insertions.

7.1.8 Module Control and Status Registers

The below registers are implemented, and can be checked for module State and Control.

	Access Type	*Bit*	*Bit Field Name*	*Description*
0xA010			***Module General Control***	
	RW	14	Soft Module Low Power	Register bit for module low power function. 1: Assert.
	RW	13	Soft TX Disable	Register bit for TX Disable function. 1: Assert.
	RW	12	Soft PRG_CNTL3 Control	Register bit for PRG_CNTL3 control function. 1: Assert.
	RW	11	Soft PRG_CNTL2 Control	Register bit for PRG_CNTL2 control function. 1: Assert.
	RW	10	Soft PRG_CNTL1 Control	Register bit for PRG_CNTL1 control function. 1: Assert.
	RW	9	Soft GLB_ALRM Test	Command bit for software forced test signal. When this bit is asserted it generates GLB_ALRM signal. 1: Assert.
	RO	8~6	Reserved	
	RO	5	TX_DIS Pin State	Logical state of the TX_DIS pin. 1: Assert.
	RO	4	MOD_LOPWR Pin State	Logical state of the MOD_LOPWR pin. 1: Assert.
	RO	3	PRG_CNTL3 Pin State	Logical state of the PRG_CNTL3 pin. 1: Assert.
	RO	2	PRG_CNTL2 Pin State	Logical state of the PRG_CNTL2 pin. 1: Assert.
	RO	1	PRG_CNTL1 Pin State	Logical state of the PRG_CNTL1 pin.
0xA016			**Module State**	
		15~9	Reserved	
		8	High-Power-down State	1: Corresponding state is active. Word value = 0100h.
		7	TX-Turn-off State	1: Corresponding state is active. Word value = 0080h.
		6	Fault State	1: Corresponding state is active. Word value = 0040h.
		5	Ready State	1: Corresponding state is active. Word value = 0020h.
		4	TX-Turn-on State	1: Corresponding state is active. Word value = 0010h.
		3	TX-Off State	1: Corresponding state is active. Word value = 0008h.
		2	High-Power-up State	1: Corresponding state is active. Word value = 0004h.
		1	Low-Power State	1: Corresponding state is active. Word value = 0002h.
		0	Initialize State	1: Corresponding state is active. Word value = 0001h.

Table 10 Module Control/State Registers

7.2 ML4029 CFP2 4x25G Retimed Loopback Additional Functions

The **IN012525** from Inphi is used as Retimer chip inside the **ML4029**, Thus the CFP2 module enables all the Inphi chip capabilities to be applied.

7.2.1 PRBS Generator

All Lanes support the transmission of the following PRBS patterns :

- PRBS 7
- PRBS 9
- PRBS 15
- PRBS 23
- PRBS 31
- 40 bit user defined pattern
- square wave generated pattern

Each lane has its own pattern control register. Generator and checker pattern selections are completely independent.

7.2.2 PRBS Checker

All lanes support pattern locking and error counting of the following PRBS patterns:

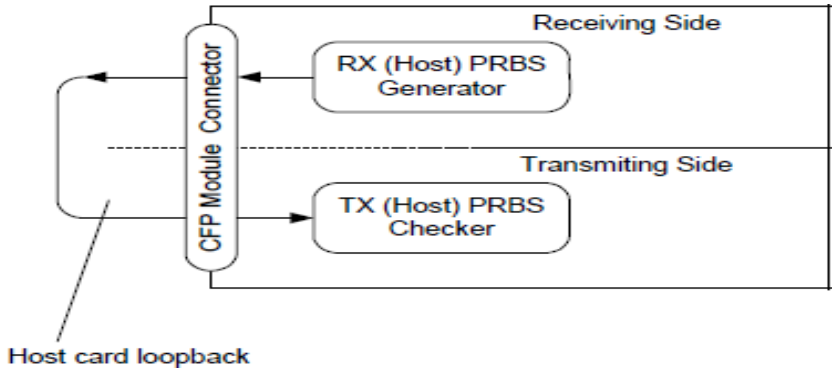
- PRBS 7
- PRBS 9
- PRBS 15
- PRBS 23
- PRBS 31

Each lane has its own pattern control register. Generator and checker pattern selections are completely independent.

7.2.3 MSA Compliant Host Lane PRBS Control

The above described PRBS Generator and checker can be controlled through MDIO by setting the corresponding CFP registers, thus CFP MSA specifies PRBS generator and error checker for each network lane with CFP register controls. To start a PRBS session, Host shall select the desired PRBS pattern by setting the bits RX PRBS Pattern 1 and RX PRBS Pattern 0 in Host Lane RX Control register (A014h.6~5). The Host enables the PRBS generators by asserting the bit RX PRBS Generator Enable in the same register (A014h.7).

Host shall apply the same operation to Host Lane Control register (A014h.13~12 and A014h.14) correspondingly to set up and enable the PRBS checker. The host side PRBS generator and checker functions shall be stopped by de-asserting the RX PRBS Generator Enable and the TX PRBS Checker Enable respectively.



7.2.4 Error Injection

The Lane Pattern control register allows the injection of error bursts into run-time data or PRBS patterns using the custom pattern register to define the burst. Writing one to the error_insert bit causes a single insertion of an error burst into the transmit data.

Error injection can be used to verify correct operation of error counters.

CFP MSA does not define registers for error injection capability, however this will still be enabled in the ML4029 by giving user direct access to the Inphi registers on the corresponding MDIO address.

7.2.5 EyeScan Capability

The eyescan function provides non destructive asynchronous eyescan, that is valid valid data receptiuon is able to continue during an eyescan.

The eyescan function provides the ability to sample incoming data at phase and voltage offsets to the current ideal sampling position used by the device.

7.2.6 Bathtub Curve Measurement

The Inphi chip allows phase shifting of the internal sampling clock allowing the checker to sample data at different phases of the incoming signal, Reading BER at each sampler position accumulates required data to perform a full bathtub curve.

7.3 ML4030 CFP2 10x10G Passive Loopback Additional Functions

7.3.1 Programmable Power Dissipation & Thermal Emulation

Register 0x8401 is used for PWM control over MDIO. It is an 8 bit data wide register.

The consumed power changes accordingly when the value in this register is changed (only when in high power mode). In Low power mode the module automatically turns off PWM.

The values written in this register can be stored by calling the Save NVR function, thus the user can permanently change the initial power consumed in high power mode when the module is powered up by setting the register value and calling the Save NVR function.

Address	Description	Data Range	Default Value
0x8401	PWM	0 to 102 (0x00 to 0x66)	0

Table 11. PWM

The PWM can also be used for module thermal emulation.

The module contains a thermal spot that can be heated relative to the related PWM register.

Note that the led starts blinking when the temperature high alarm is reached.

7.3.2 Cut-Off Temperature

To avoid overheating the module, a Cut-Off Temperature is stored in Register 0x8402.

The module is continuously monitoring the temperature and checking its value against the Cut-Off temperature, once reached the module automatically turns off PWM to avoid overheating.

The Default Cut-Off temperature for the ML4030 is 85 degC, so even if the value stored in register 0x8402 is higher than 85 the module will still Cut-Off power at 85 degC, in case the value stored in 0x8402 is lower than 85 then it will be adopted instead of the default value.

Address	Description	Data Range	Default Value
0x8402	Cut-Off Temperature	0 to 255 (0x00 to 0xFF)	0x55

Table 12. PWM

7.3.3 RX_LOS

In the ML4030, RX_LOS is connected to TX_DIS, so RX_LOS output is driven by TX_DIS control, this does not report the actual LOS status of the module since the loopback is passive, but can be used for testing the CFP2 port pins on the host side.

7.4 ML4043 CFP2 10x10G Retimed Loopback Additional Functions

The **VSC7227** from Vitesse is used as Retimer chip inside the **ML4043**, Thus the CFP2 module enables all the VSC capabilities to be applied.

7.4.1 Input Equalization

The VSC7227 device features a front end adaptive input equalizer stage. The input signal equalization on the VSC 7227 device helps to combat the Inter Symbol Interference(ISI) of High-speed data as it passes through lossy media. The VSC7277 device provides flexibility in correcting for transmission losses by providing six independent equalization stages.

CFP MSA does not specify registers for such functionality, However it is provided on the ML4043 by providing direct access to the VSC7227 on corresponding MDIO address (address to be defined later).

7.4.2 Input and DFE Adaptation

ML4043 enables optimal compensation of copper losses in backplanes, copper traces and cables, additional control is provided through MDIO interface (Registers to be defined later) to adapt the equalizer settings on the Vitesse for custom signal compensation.

The DFE tap settings on the Vitesse auto adapts to compensate for crosstalk and reflection, custom control is also provided thru MDIO interface for custom adaptation.

7.4.3 Loss of Signal (LOS) Detection

The Receiver Loss of Signal Pin (RX_LOS) is an output pin to the Host, operating with active-high logic. When asserted, it indicates received power in the CFP2 module is lower than the expected value (RX in this application is considered to be the RX pins of the CFP2 connector, so it is a Host side Loss of Signal Detection).

When the incoming signal strength goes below the programmed threshold value, the LOS signal is asserted.

The corresponding registers specified by CFP MSA are implemented to store the RX_LOS status for each Host Lane (Registers to be defined later).

7.4.4 Clock Recovery Unit

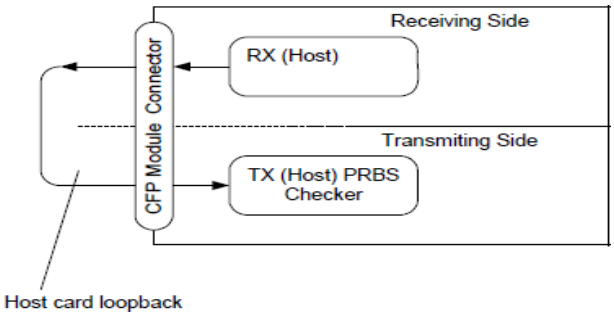
The VSC7227 device performs clock recovery on the incoming input pins. The recovered clock is used by the data recovery block to regenerate the data by sampling the output of the summing circuit. The data recovery section samples the waveform at the optimal phase and sets the output bit either high or low.

7.4.5 Host Lane PRBS Checker

A PRBS error checker is implemented for each Host lane with CFP register controls. To start a PRBS session, Host shall select the desired PRBS pattern by setting the bits RX PRBS Pattern 1 and RX PRBS Pattern 0 in Host Lane Control register (A014h.6~5).

The Host enables the TX PRBS checker by asserting the bit in Host Lane Control register (A014h.14).

The host side PRBS checker function shall be stopped by de-asserting the TX PRBS Checker Enable respectively.



8. ML4027/ML4027-ACO/ML4042 CFP2 Host Programming Manual

8.1 Introduction

This part of the manual describes the key features, the GUI that is used to communicate with the **ML4027/ML4042** MSA Compliant CFP2 Host Boards for testing and characterizing any MSA Compliant CFP2 module when plugged into the Host.

In the following context we will be describing the GUI communication with ML4042 having 10 channels, the same concept applies to ML4027 but only 4 channels [3:0] are considered.

8.1.1 Key Features

ML4042

- 10 TX & 10 RX Lanes, high-speed signals accessible through 40 SMAs, 18GHz connectors.
- High performance Signal Integrity traces from coax to interface.
- Operates up to 11.2 Gbps per channel
- User Friendly GUI for MDIO control and loading MSA tables.
- CFP Host/ Module Status and control.
- USB controlled.
- MSA compliant Digital Diagnostic and Monitoring Interface (DDMI).
- Status LEDs indicators for signal monitoring and MSA defined Alarms.
- Onboard jumpers for MSA defined control signals.
- Onboard & external reference clock (SMP)
- Built with advanced Rogers™ material.
- DCS (de-skew) lane (2 SMP).

ML4027

- 4 TX & 4 RX Lanes, high-speed signals accessible through 16 Southwest End Launch Super SMA 27GHz connectors.
- High performance Signal Integrity traces from coax to interface.
- Operates up to 28 Gbps per channel
- User Friendly GUI for MDIO control and loading MSA tables.
- CFP Host/ Module Status and control.
- USB controlled.
- MSA compliant Digital Diagnostic and Monitoring Interface (DDMI).

- Status LEDs indicators for signal monitoring and MSA defined Alarms.
- Onboard jumpers for MSA defined control signals.
- Onboard & external reference clock (SMP)
- Built with advanced Rogers™ material.
- DCS (de-skew) lane (2 SMP).

8.1.2 Benefits

- Economical CFP2 Port Testing
- Custom Memory Maps
- Board Level System Testing

8.1.3 Applications

Electro-Optical module testing and Characterization

8.1.4 Software Capabilities

- CFP Module Status/ Control
- MSA Compliant
- DDMI

8.1.5 Power Requirements

The CFP2 Host module is powered using an external **5V** source .

8.2 Package Contents

The **ML4027/ML4042** product includes the following:

1. The CFP2 Passive Host fixture.
2. The software package:

   One Installer package to automatically install the GUI along with required drivers for the Host.

The GUI runs under Windows XP SP3 (32/64 bits), Vista and Windows 7 OS.

NOTE. *The CFP2 Host GUI application requires the* ***Microsoft .NET Framework 4*** *. If the Microsoft .NET Framework 4 is not existing on your PC, it can be downloaded through this link:*
http://www.microsoft.com/en-us/download/details.aspx?id=24872

This CFP2 Host software controls the CFP2 Host fixture through USB. The USB drivers will be installed directly with the software installation. In case automatic driver installation failed, you have to install them manually. Please refer to the section **USB Driver installation on Windows XP**.
Remember to connect the PC to the fixture through a usb cable.

8.3 Installation

8.3.1 USB Driver Installation on Windows XP

- Power on the CFP2 Host fixture.
- Plug-in the USB cable into the PC and connect it to the CFP2 Host fixture.
- The following window will pop up.
- Choose the "**No, not this time**" option, and then click "**Next**".

Figure 5: USB driver installation

- Choose "**Install from a list or specific location (Advanced)**", and then click "**Next"**.

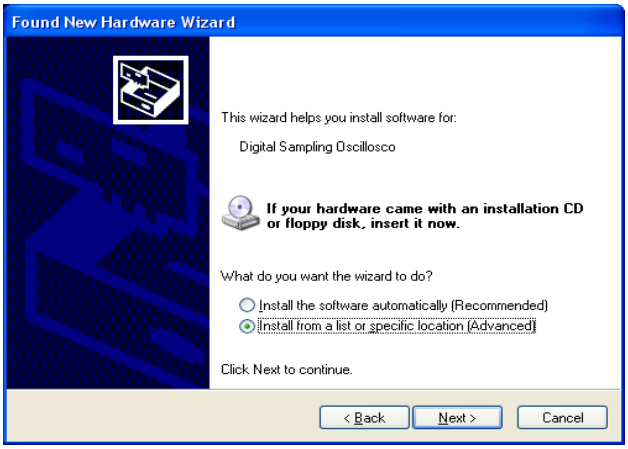


Figure 6: USB driver installation Advanced

- Choose "**Search for the best driver in these locations**".
- Check the choice: "**Include this location in the search**".
- Browse for the subfolder: "**CFP Host**" existing in "**MultiLane Drivers**" folder in the installation path. Choose it and then click **"Ok"**.
- Click "**Next**".

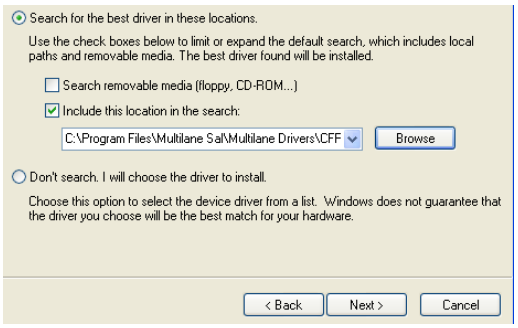


Figure 7: USB driver location

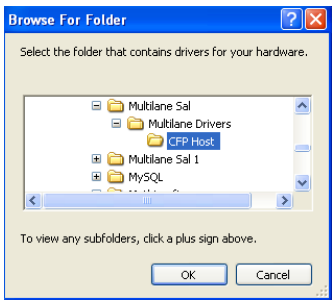


Figure 8: USB driver folder

- When this window appears, click "**Finish**". The USB driver is now installed.

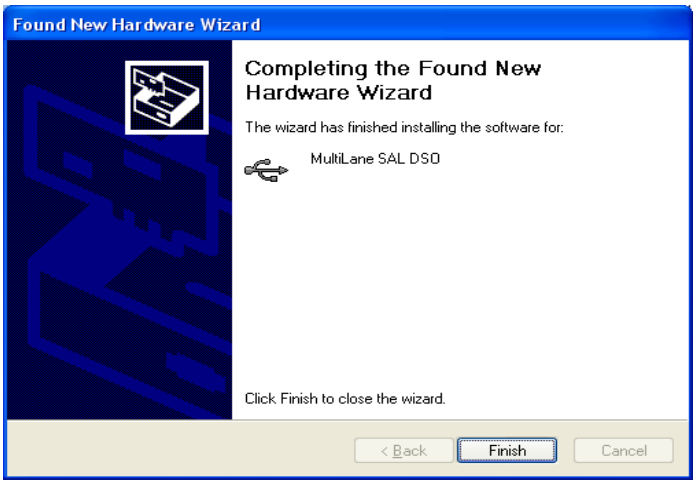


Figure 9: USB driver installation Finish

8.5 Communication Window

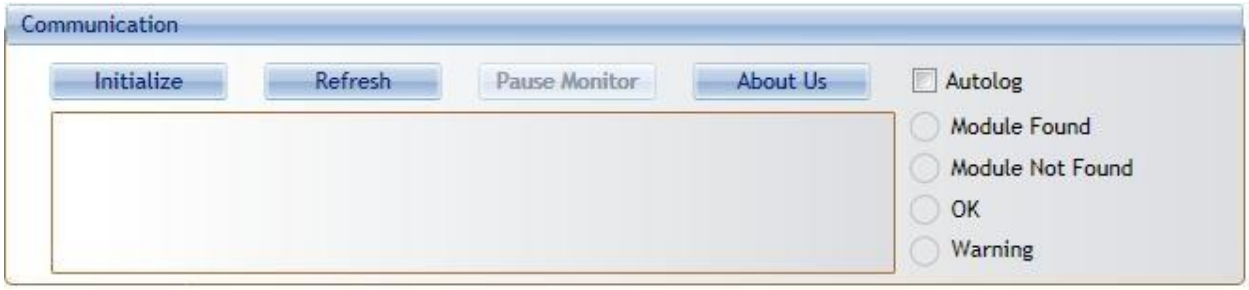


Figure 10 Communication Window: Main Interface used for initial communication with host

The Initialize button is the application's main entry point, used to establish a connection with the CFP2 Host board and the Module. Once a USB connection is established, the Host checks if a CFP2 Module is inserted, and accordingly illuminates the corresponding (Module Found or Module Not Found) LED. If a CFP2 Module is inserted, the initialization process proceeds with the MSA compliant startup sequence for the module as shown in the diagram below:

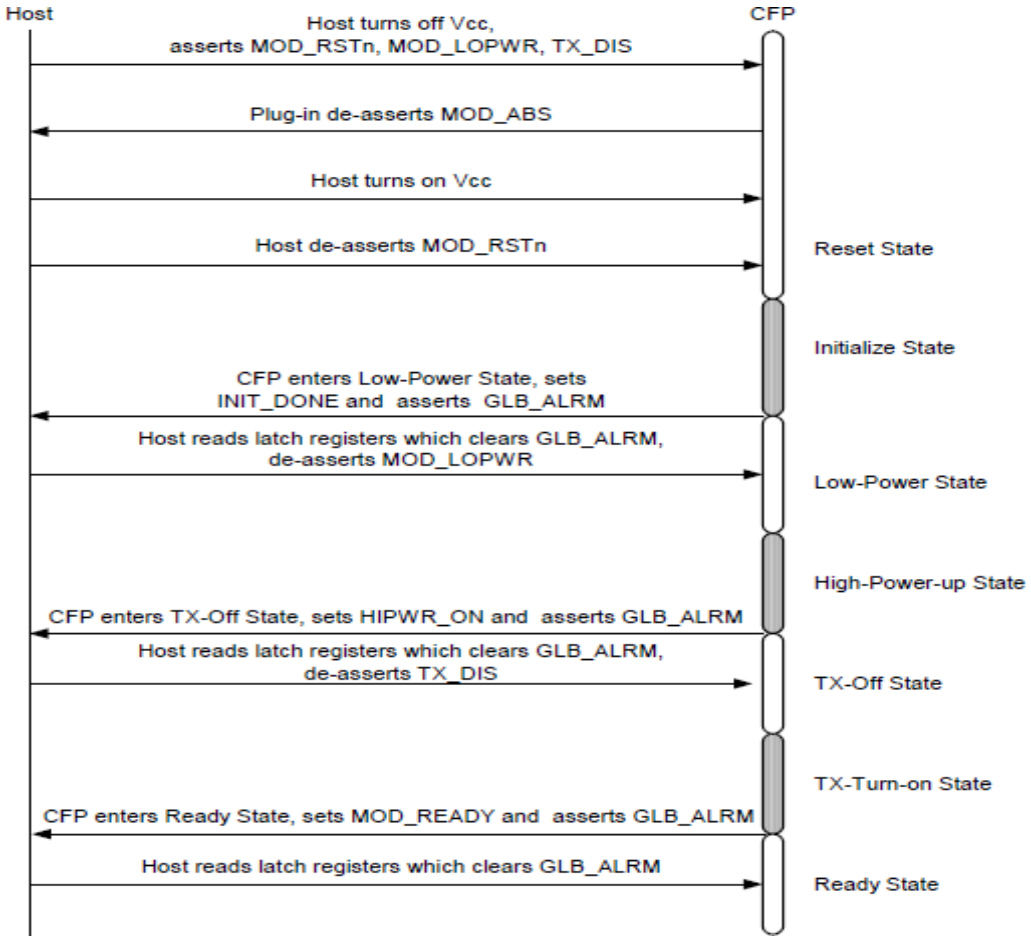


Figure 11 MSA Compliant Startup Sequence

Hence, the CFP2 module goes through Reset, Initialize, High-Power up, TX-Off, TX-Turn-on states, and finally enters the Ready state. During this sequence, the CFP2 module sets INIT_DONE, asserts GLB_ALRM, HIPWR_ON, and MOD_READY signals sequentially. These signals inform host the completion of control circuit initialization and MDIO availability, module fully powered up, and module ready for data, respectively. OK LED will be asserted when the module startup sequence is complete.

Next, the status box window in the GUI will show any success or failure messages that are being returned as a result of the GUI communicating or attempting to communicate with the hardware.

Figure 12 Communication status box showing a connection error

The above figure shows a typical connection error when a connection attempt with the host fails. The default Error Status format is: [funtion]:[returned error].

The picture below shows how the status box should appear after a successful connection.

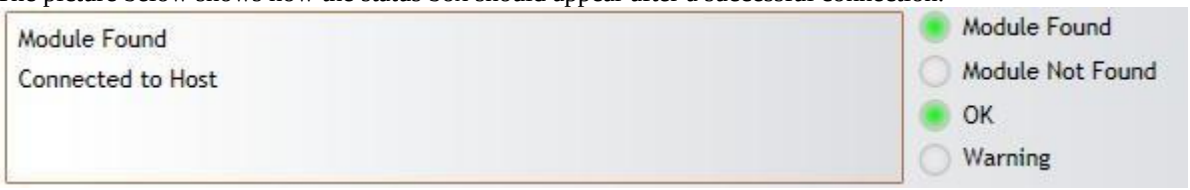


Figure 13 Communication status box showing successful connection

Figure 14 Communication status box when connected to host but no module is plugged

Please note that the status box messages are always shown with the most recent message on top. You can check the "Autolog" check box for activating the silent logging mode. In this mode, a log file will be automatically generated, and all software steps will be logged during runtime and is useful for debugging purposes when communicating with Multilane applications engineering support.

Refresh button: checks for connection status, refresh Hardware Readings and updates GUI

Pause Monitor button: Pause/Resume monitoring.

About Us button: shows program information (name, version) and company information.

8.6 Graphical User Interface Section

The GUI for the CFP2 host board contains 13 sections giving the user the ability to monitor, customize, control and configure the Hardware.

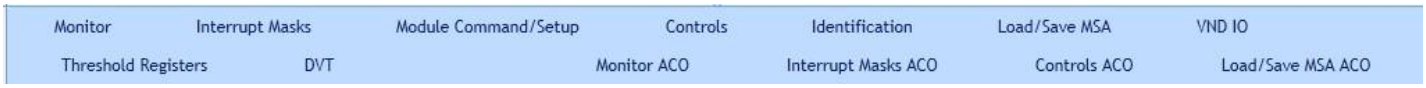


Figure 15 GUI tabs

As shown in Figure 15 above, the GUI contains the following main tabs:

- ✓ **Monitor/Monitor ACO**: Monitoring interface allowing the user to check the Hardware operation.
- ✓ **Interrupt Masks/Interrupt Masks ACO**: Allows the user to select which FAWS bits to contribute to GLB_ALRM.
- ✓ **Module Command/Setup**: Allows the user to control module behavior.
- ✓ **Controls/Controls ACO**: Provides both additional and alternative controls to hardware pins and programmable control pins in controlling CFP2 module.
- ✓ **5-Identification:** Shows module Base ID Registers.
- ✓ **6-Load-Save MSA/Load-Save MSA ACO:** Save the current CFP2 configuration to a file, or load existing configuration from file and map it to MSA memory.
- ✓ **7-VND IO:** Provides control for CFP Vendor IO pins.

As noticed, this GUI supports both ML4027 CFP2 Host and ML4027-ACO CFP2-ACO Host.

To enable ACO mode, the user should check the below ACO Checkbox. When it's checked, the related tabs are shown and the unrelated tabs are hidden.

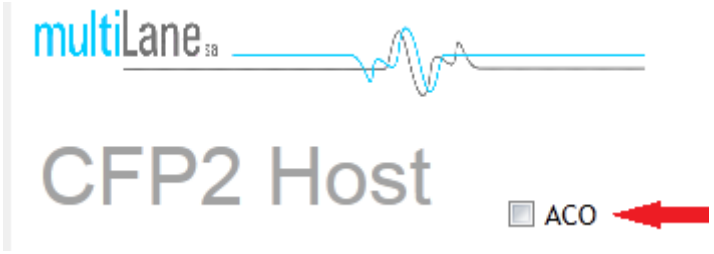


Figure 16. ACO option

8.6.1 Monitor

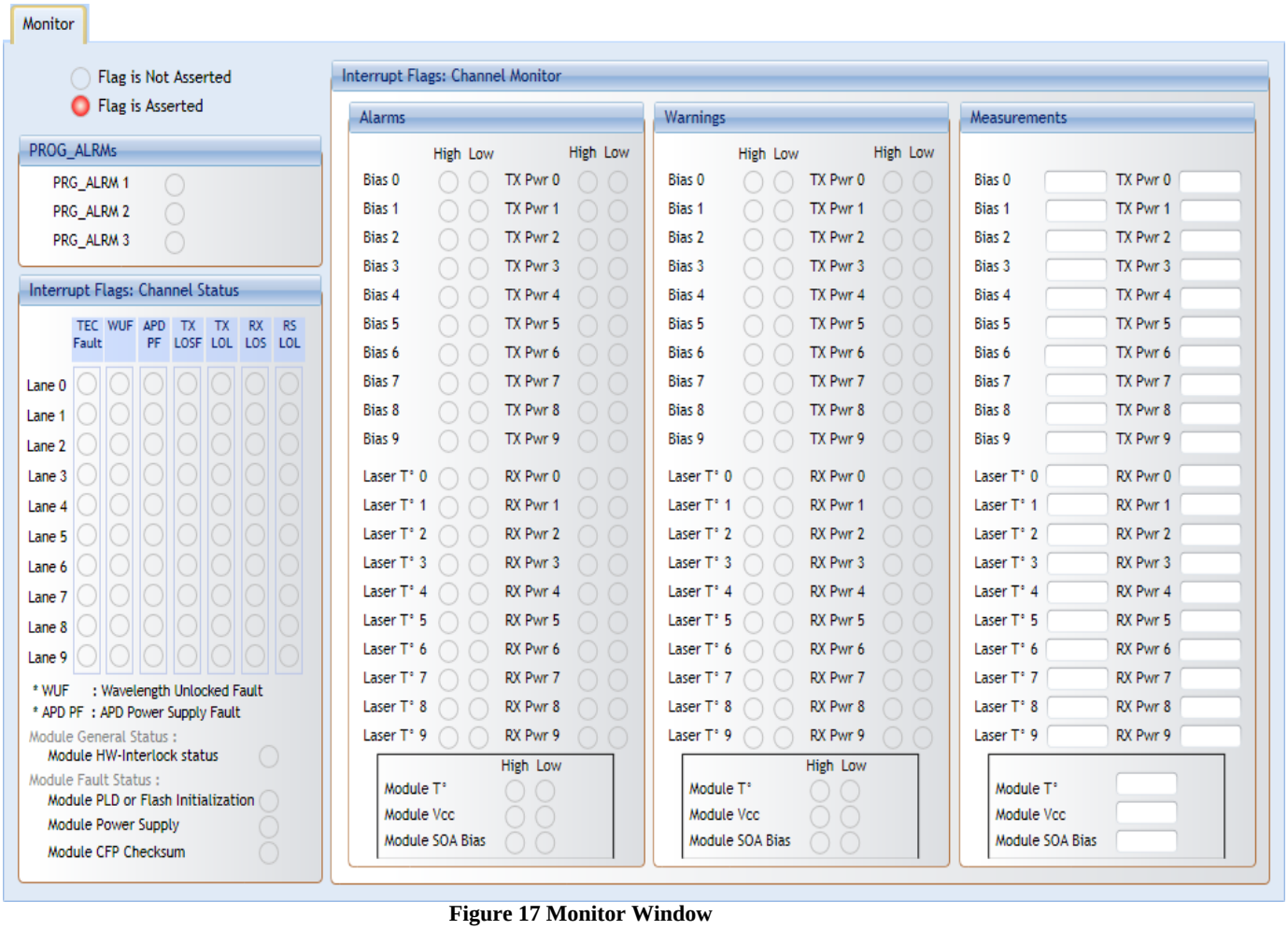


Figure 17 Monitor Window

Digital Diagnostic Monitor:

The Monitor Window shown in Figure 16 above is the main source of the module status and alarm/warning flags conditions. It shows the current status of a flag, the default flag update rate is 2 Hz, so the flag status is updated every 0.5 seconds.

Flag Status:

- Flag is not asserted: the corresponding LED is OFF (Transparent).
- Flag is asserted: the corresponding LED is ON (Red).

The Monitor window shows 3 different sections:

1- PRG_ALRMs

2- Interrupt Flags: Channel Status

3- Interrupt Flags: Channel Monitor

8.6.1.1 PRG_ALRMS

Figure 18 PRG_ALRMs window

PRG_ALRM1, PRG_ALRM2 and PRG_ALRM3 are programmable alarm pins that can be programmed with custom alarm sources. When the custom select alarm is enabled, the corresponding LED is asserted on the monitor screen. Please refer to section 3.3-II for information about how to set a custom alarm source for PRG_ALRMs.

8.6.1.2 Interrupt Flags: Channel Status

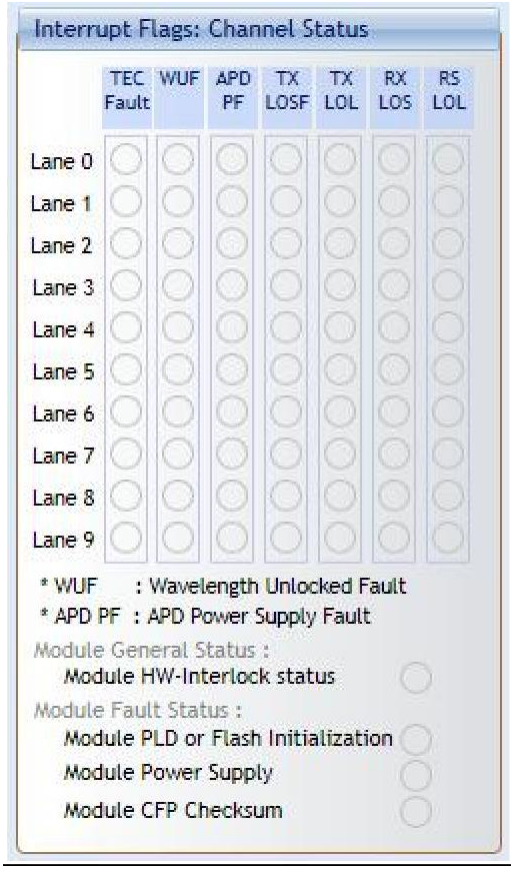


Figure 19 Interrupt Flags: Channel Status Window

I- Network Lane n Fault and Status

A210	16	RO		Network Lane n Fault and Status	16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent.	0000h
			15	Lane TEC Fault	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
			14	Lane Wavelength Unlocked Fault	0: Normal; 1: Asserted. (FAWS_TYPE_C)	0
			13	Lane APD Power Supply Fault	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
			12~8	Reserved		0
			7	Lane TX_LOSF	0: Normal; 1: Asserted. (PMD) (FAWS_TYPE_C)	0
			6	Lane TX_LOL	0: Normal; 1: Asserted. (Network) (FAWS_TYPE_B)	0
			5	Reserved		0
			4	Lane RX_LOS	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
			3	Lane RX_LOL	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
			2~0	Reserved		000b

Figure 20 CFP MSA memory map for Network Lane n Fault and Status registers

Figure 21 Network Lane n Fault and Status corresponding LEDs

The above picture shows the status LEDs of the flags shown in Figure 19. When a flag is asserted, the corresponding LED is illuminated red.

II- Module Fault and Status

Module FAWS Registers						
A01D	1	RO		**Module General Status**		**0000h**
			15	Reserved		0
			14	Reserved		0
			13	HW_Interlock	Module internally generated status signal. (FAWS_TYPE_A) 0: If module power <= Host cooling capacity or if hardware Interlock is not used, 1: If module power > Host cooling capacity.	0
A01E	1	RO		**Module Fault Status**	**Module Fault Status bit pattern. Only fatal faults that are potentially harmful to the module can trigger the bits here. All the bits are 0: Normal; 1: fault detected. When any bit in this register is a '1', The Module State register will also be set to the Fault State.**	**0000h**
			15~7	Reserved		0
			6	PLD or Flash Initialization Fault	PLD, CPLD, or FPGA initialization fault. (FAWS_TYPE_A)	0
			5	Power Supply Fault	1: Power supply is out of range. (FAWS_TYPE_A)	0
			4~2	Reserved		000b
			1	CFP Checksum Fault	1: CFP Checksum failed. (FAWS_TYPE_A)	0
			0	Reserved		0

Figure 22 CFP MSA Module General Status and FAWS Registers

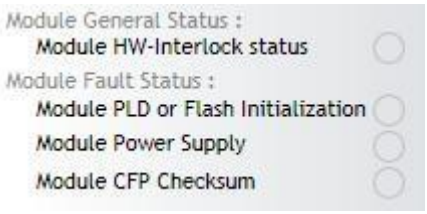


Figure 23 Module General Status and Fault corresponding LEDs

The above window represents the status LEDs of flags shown in Figure 21. When a flag is asserted, the corresponding LED is illuminated red.

8.6.1.3 *Interrupt Flags: Channel Monitor*

I- Network Lane Alarms and Warnings

A200	16	RO		Network Lane n Alarm and Warning	16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent.	0000h
			15	Bias High Alarm	0: Normal; 1: Asserted. (FAWS_TYPE_C)	0
			14	Bias High Warning	0: Normal; 1: Asserted. (FAWS_TYPE_C)	0
			13	Bias Low Warning	0: Normal; 1: Asserted. (FAWS_TYPE_C)	0
			12	Bias Low Alarm	0: Normal; 1: Asserted. (FAWS_TYPE_C)	0
			11	TX Power High Alarm	0: Normal; 1: Asserted. (FAWS_TYPE_C)	0
			10	TX Power High Warning	0: Normal; 1: Asserted. (FAWS_TYPE_C)	0
			9	TX Power Low Warning	0: Normal; 1: Asserted. (FAWS_TYPE_C)	0
			8	TX Power Low Alarm	0: Normal; 1: Asserted. (FAWS_TYPE_C)	0
			7	Laser Temperature High Alarm	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
			6	Laser Temperature High Warning	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
			5	Laser Temperature Low Warning	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
			4	Laser Temperature Low Alarm	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
			3	RX Power High Alarm	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
			2	RX Power High Warning	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
			1	RX Power Low Warning	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
			0	RX Power Low Alarm	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0

Figure 24 Network Lane n Alarm and Warning Registers

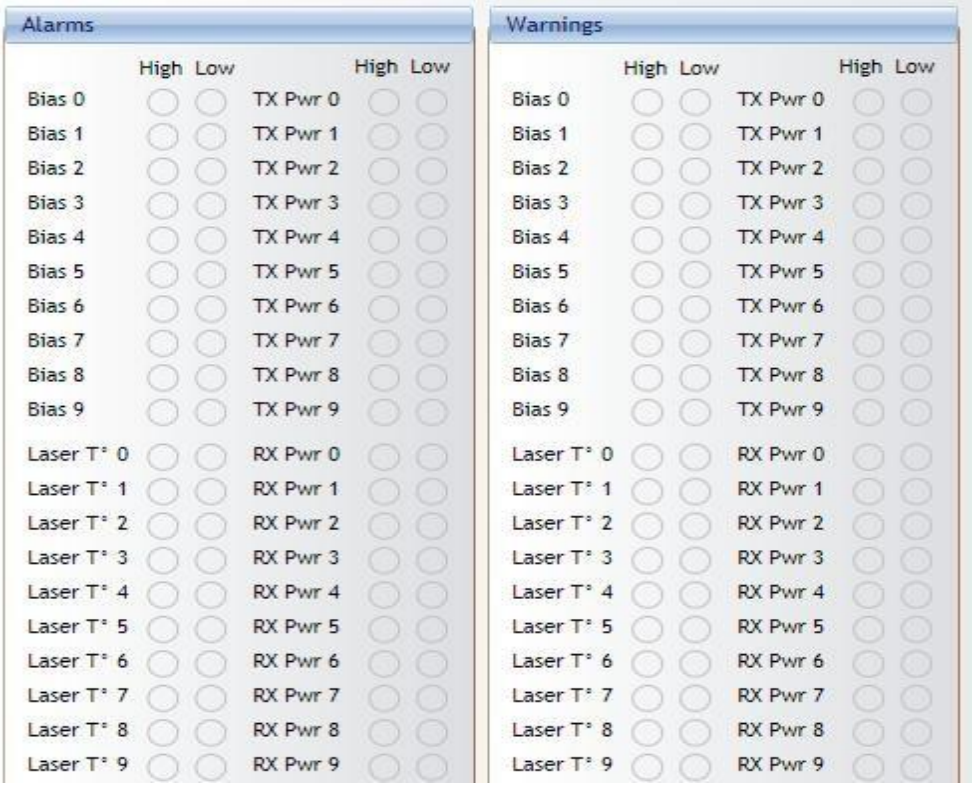


Figure 25 Network Lane n Alarms and Warnings LEDs

The above windows represent the status LEDs of flags shown in fig 23. There are 4 alarms/warnings that are defined as follows: Laser Bias Current, Laser Temperature, Laser Output Power and Receiver Input Power. When a flag is asserted, the corresponding LED is illuminated red.

II- Module Alarms and Warnings

A01F	1	RO		Module Alarms and Warnings 1		0000h
			15~12	Reserved		0000b
			11	Mod Temp High Alarm	Mod temp high Alarm. (FAWS_TYPE_A) 0:Normal, 1:Alarm assert.	0
			10	Mod Temp High Warning	Mod temp high Warning. (FAWS_TYPE_A) 0:Normal, 1:Warning assert	0
			9	Mod Temp Low Warning	Mod temp low Warning. (FAWS_TYPE_A) 0:Normal, 1:Alarm assert	0
			8	Mod Temp Low Alarm	Mod temp low Alarm. (FAWS_TYPE_A) 0:Normal, 1:Warning assert	0
			7	Mod Vcc High Alarm	Input Vcc high Alarm. (FAWS_TYPE_A) 0:Normal, 1:Alarm assert	0
			6	Mod Vcc High Warning	Input Vcc high Warning. (FAWS_TYPE_A) 0:Normal, 1:Alarm assert	0
			5	Mod Vcc Low Warning	Input Vcc low Warning. (FAWS_TYPE_A) 0:Normal, 1:Alarm assert	0
			4	Mod Vcc Low Alarm	Input Vcc low Alarm. (FAWS_TYPE_A) 0:Normal, 1:Alarm assert	0
			3	Mod SOA Bias High Alarm	SOA bias current high alarm. (FAWS_TYPE_B) 0:Normal, 1:Alarm assert	0
			2	Mod SOA Bias High Warning	SOA bias current high warning. (FAWS_TYPE_B) 0:Normal, 1:Alarm assert	0
			1	Mod SOA Bias Low Warning	SOA bias current low warning. (FAWS_TYPE_B) 0:Normal, 1:Alarm assert	0
			0	Mod SOA Bias Low Alarm	SOA bias current low alarm. (FAWS_TYPE_B) 0:Normal, 1:Alarm assert	0

Figure 26 Module Alarms and Warnings Register

Figure 27 Module Alarms and Warnings LEDs

The above section represents the status LEDs of flags shown in figure 25.

III- Measurements

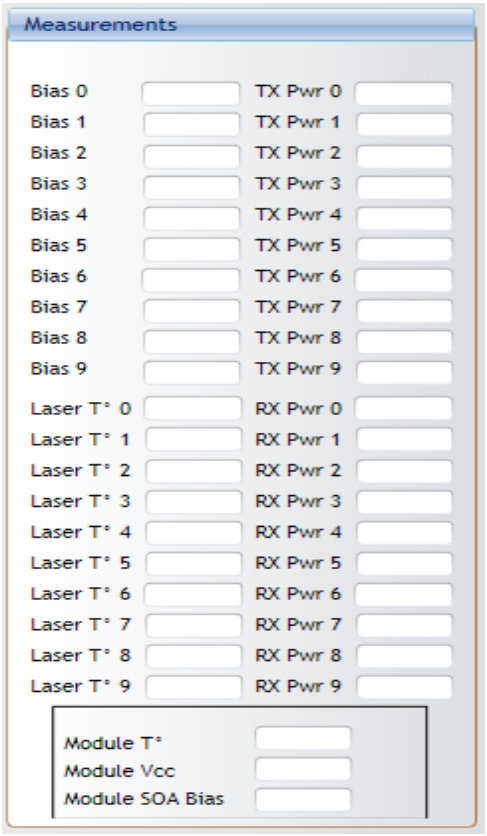


Figure 28 Measurement window

Network Lane n A2D measurements:

Network Lane n Laser Bias Current monitor A2D value: Measured laser bias current, representing a total measurement range of 0 to 131.072 mA.

Network Lane n Laser Output Power monitor A2D value: Measured TX output power, representing a range of laser output power from 0 to 6.5535 mW.

Network Lane n Laser Temp Monitor A2D value: Internally measured temperature in degrees Celsius.

Network Lane n Receiver Input Power monitor A2D value: Measured received input power, representing a power range from 0 to 6.5535 mW.

Module A2D value measurements:

Three analog values, Module Temperature Monitor A/D Value, Module Power Supply 3.3V Monitor A/D Value, and SOA Bias Current A/D Value are measured.

These monitoring values are at the module level and non-network lane specific. The values in these registers are automatically updated by the CFP2 module every 100ms.

8.6.2 Interrupt Masks

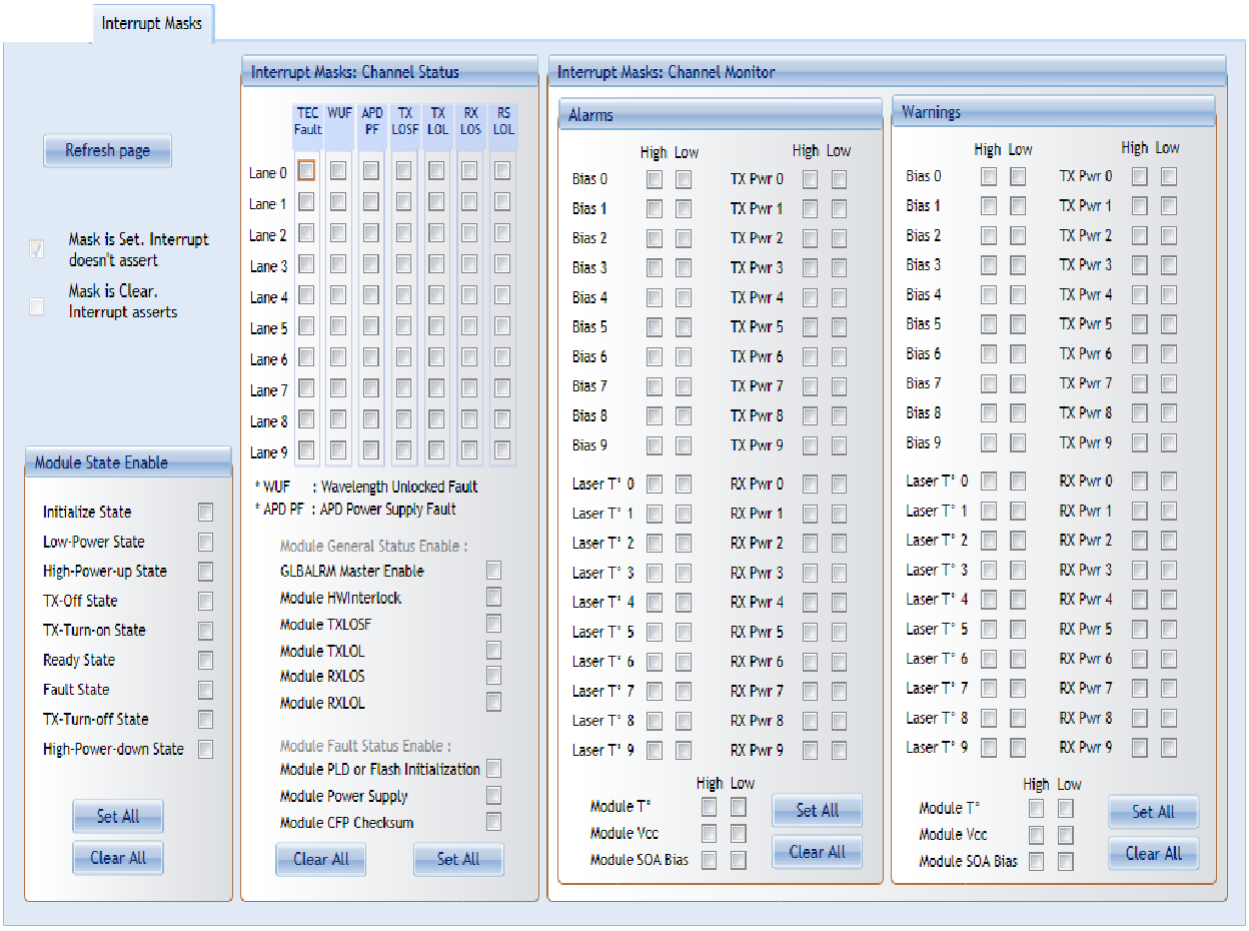


Figure 29 Interrupt Masks screen

All the check boxes provided on this screen either set or clear the corresponding FAWS Enable Registers.

The CFP2 FAWS Enable registers allows the host to enable or disable any particular FAWS bits to contribute to GLB_ALRM. When a mask bit is set, the corresponding alarm or warning will not contribute in triggering the Global Alarm. When a mask is cleared, then the assertion of an alarm or warning will trigger the Global Alarm.

8.6.3 Module Command/Setup

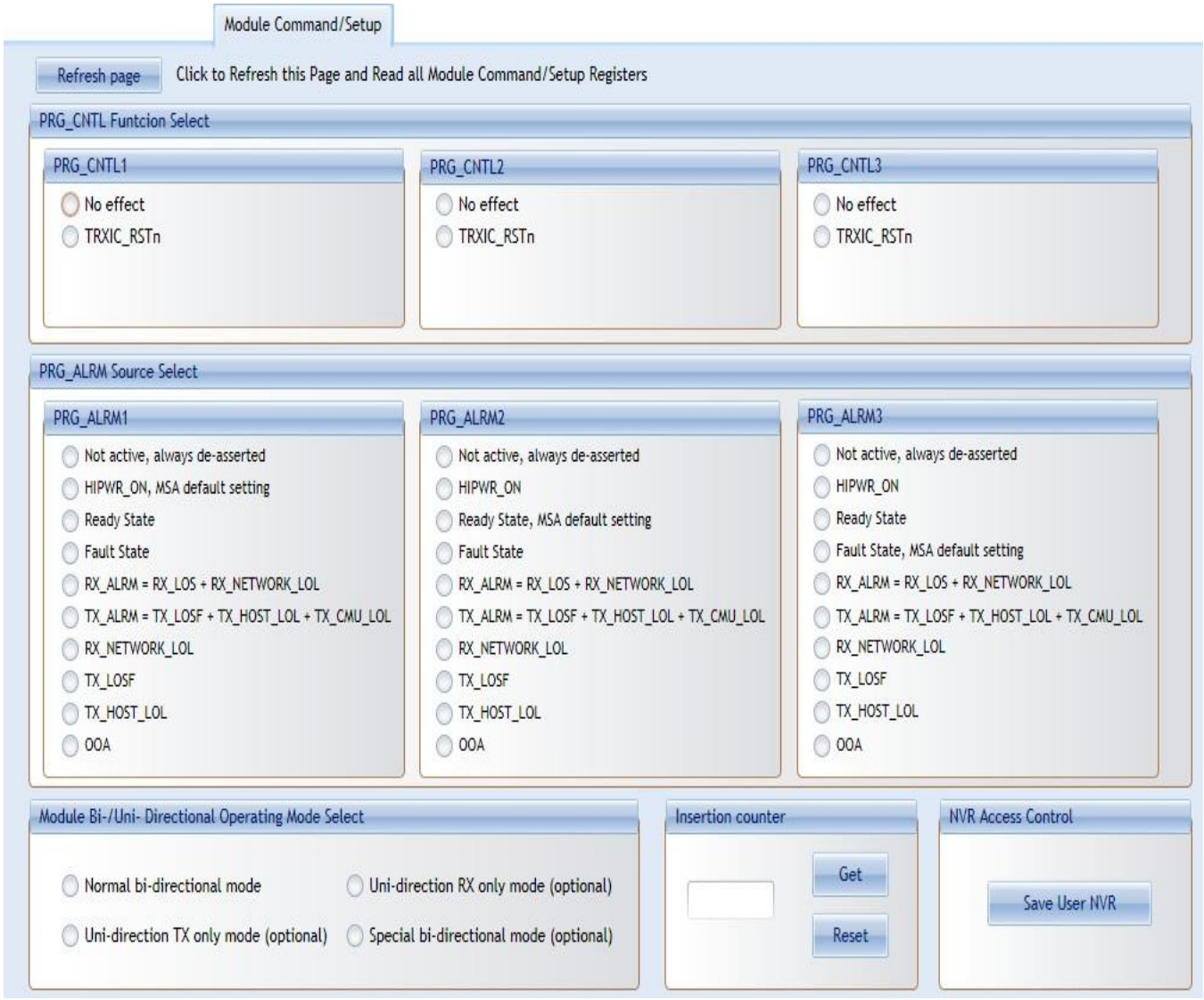


Figure 30 Module Command/Setup screen

This above screen allows customizing some registers that the host uses to control actual module behavior. Through this screen, the user can select a custom control function for the PRG_CNTL hardware pin, or select a custom source for the PRG_ALRM hardware pin alarm, and will also be able to define a module operating mode.

I- PRG_CNTLs Function Select

A005	1			PRG_CNTL3 Function Select	Selects, and assigns, a control function to PRG_CNTL3.	0000h
		RO	15~8	Reserved		00h
		RW	7~0	Function Select Code	This multi-function input is used as HW_IL_MSB during the Initialize State and it can be programmed to other functions afterward. 0: No effect, 1: Assign TRXIC_RSTn function to hardware pins PRG_CNTL3. When so assigned this pin uses the active low logic, that is, 0 = Assert (Reset). Note that when so assigned, its soft counterpart Soft PRG_CNTL3 Control (A010h.12) uses an active high logic, that is, 1 = Assert (Reset). 2~255: Reserved.	00h
A006	1			PRG_CNTL2 Function Select	Selects, and assigns, a control function to PRG_CNTL2.	0000h
		RO	15~8	Reserved		00h
		RW	7~0	Function Select Code	This multi-function input is used as HW_IL_LSB during the Initialize State and it can be programmed to other functions afterward. 0: No effect, 1: Assign TRXIC_RSTn function to hardware pins PRG_CNTL2. When so assigned this pin uses the active low logic, that is, 0 = Assert (Reset). Note that when so assigned, its soft counterpart Soft PRG_CNTL2 Control (A010h.11) uses an active high logic, that is, 1 = Assert (Reset). 2~255: Reserved.	00h
A007	1			PRG_CNTL1 Function Select	Selects, and assigns, a control function to PRG_CNTL1.	0001h
		RO	15~8	Reserved		00h
		RW	7~0	Function Select Code	0: No effect, 1: Assign TRXIC_RSTn function to hardware pins PRG_CNTL1. When so assigned this pin uses the active low logic, that is, 0 = Assert (Reset). Note that when so assigned, its soft counterpart Soft PRG_CNTL1 Control (A010h.10) uses an active high logic, that is, 1 = Assert (Reset). TRXIC_RSTn is the CFP MSA default function for PRG_CNTL1. 2~255: Reserved.	01h

Figure 31 CFP MSA PRG_CNTLs Function Select (A005h, A006, A007h) registers

The registers shown in Figure 30 select a control function for the programmable control pins. Each programmable control pin can be programmed with the functions as defined below.

NAME	FUNCTION	VALUE
TRXIC_RSTn	Reset TX and RX ICs, PRG_CNTL1 MSA default.	0: Normal, 1: Assign TRXIC_RSTn function to any of the 3 hardware pins PRG_CNTL3, PRG_CNTL2, and PRG_CNTL1. When so assigned these hardware pins use the active low logic, that is, 0 = Assert (Reset). Note that when so assigned, their soft counterparts Soft PRG_CNTL3, Soft PRG_CNTL2, and Soft PRG_CNTL1 (A010h.12~10) use an active high logic, that is, 1 = Assert (Reset).

Figure 32 Programmable Control Functions

II- PRG_ALRMs Source Select

A008	1			PRG_ALRM3 Source Select	**Selects, and assigns, an alarm source for PRG_ALRM3.**	0003h
		RO	15~8	Reserved		00h
		RW	7~0	Alarm Source Code	0: Not active, always de-asserted, 1: HIPWR_ON, 2: Ready State, 3: Fault State, MSA default setting, 4: RX_ALRM = RX_LOS + RX_NETWORK_LOL, 5: TX_ALRM = TX_LOSF + TX_HOST_LOL + TX_CMU_LOL, 6: RX_NETWORK_LOL, 7: TX_LOSF, 8: TX_HOST_LOL, 9: OOA, Out of alignment, (Only applicable to certain products. If not implemented in the module, Writing 9 to this register has no effect and shall be read as 0. This is also true for Registers A009h and A00Ah). 10~255: Reserved.	03h
A009	1			PRG_ALRM2 Source Select	**Selects, and assigns, an alarm source for PRG_ALRM2.**	0002h
		RO	15~8	Reserved		00h
		RW	7~0	Alarm Source Code	0: Not active, always de-asserted, 1: HIPWR_ON,	02h
					2: Ready State, MSA default setting, 3: Fault State, 4: RX_ALRM = RX_LOS + RX_NETWORK_LOL, 5: TX_ALRM = TX_LOSF + TX_HOST_LOL + TX_CMU_LOL, 6: RX_NETWORK_LOL, 7: TX_LOSF, 8: TX_HOST_LOL, 9: OOA, Out of alignment, refer to description of A008h for details, 10~255: Reserved.	
A00A	1			PRG_ALRM1 Source Select	**Selects, and assigns, an alarm source for PRG_ALRM1.**	0001h
		RO	15~8	Reserved		00h
		RW	7~0	Alarm Source Code	0: Not active, always de-asserted, 1: HIPWR_ON, MSA default setting, 2: Ready State, 3: Fault State, 4: RX_ALRM = RX_LOS + RX_NETWORK_LOL, 5: TX_ALRM = TX_LOSF + TX_HOST_LOL + TX_CMU_LOL, 6: RX_NETWORK_LOL, 7: TX_LOSF, 8: TX_HOST_LOL, 9: OOA, Out of alignment, refer to description of A008h for details, 10~255: Reserved.	01h

Figure 33 CFP MSA PRG_ALRMs Source Select (A008h, A009h, A00Ah) registers

Each of the registers in Figure 32 select an alarm source for the programmable alarm pins. Each programmable alarm pin can be programmed with the alarm sources defined below.

NAME	ALARM SOURCE	VALUE
HIPWR_ON	Module high-power-on indicator. PRG_ALRM1 MSA default.	0: Module not high powered up, 1: Module high power up completed.
MOD_READY	MOD_READY, module startup sequence done, PRG_ALRM2 MSA default.	0: Not done, 1: Done.
MOD_FAULT	Fault detected. PRG_ALRM3 MSA default.	0: No Fault, 1: Fault.
RX_ALRM	Receive path alarm = RX_LOS + RX_LOL.	0: No receive path alarm, 1: Receive path alarm asserted.
TX_ALRM	Transmit path alarm = TX_LOSF + TX_HOST_LOL + TX_CMU_LOL.	0: No transmit path alarm, 1: Transmit path alarm asserted.
RX_LOL	RX IC Lock Indicator.	0: Locked, 1: Loss of lock.
TX_LOSF	Transmitter Loss of Signal Functionality.	0: All transmitter signals functional, 1: Any transmitter signal not functional
TX_LOL	TX IC Lock Indicator.	0: Locked, 1: Loss of lock.
OOA	Host lane skew out of alignment indicator.	0: No OOA, 1: Out of alignment.

Figure 34 Programmable Alarm Sources

III - Module Bi-/Uni Directional Operating mode select

A00B	**1**			**Module Bi-/Uni-Directional Operating Mode Select**		**0000h**
		RO	15~3	Reserved		0
		RW	2~0	Module Bi/uni-direction mode Select	000b: Normal bi-directional mode, 001b: Uni-direction TX only mode (optional), 010b: Uni-direction RX only mode (optional), 011b: Special bi-directional mode (optional), 100b~111b: Reserved.	000b

IV- Insertion Counter (Multilane CFP2 Modules specific)

This feature is implemented in the ML4029,ML4030 and ML4043 CFP2 loopback modules; it shows the insertion counter saved in register 0x8400, user can reset this counter to zero (typical reset duration ~2 sec)

V- NVR Access Control

Button Save User NVR will write 0x0020 to register A004 causing the NVR registers to be saved to NVM storage. Use this function with ML4029,ML4030 and ML4043 CFP2 loopback modules in order to save non volatile registers to the module's Flash memory.(typical time wait ~ 2sec).

8.6.5 Controls

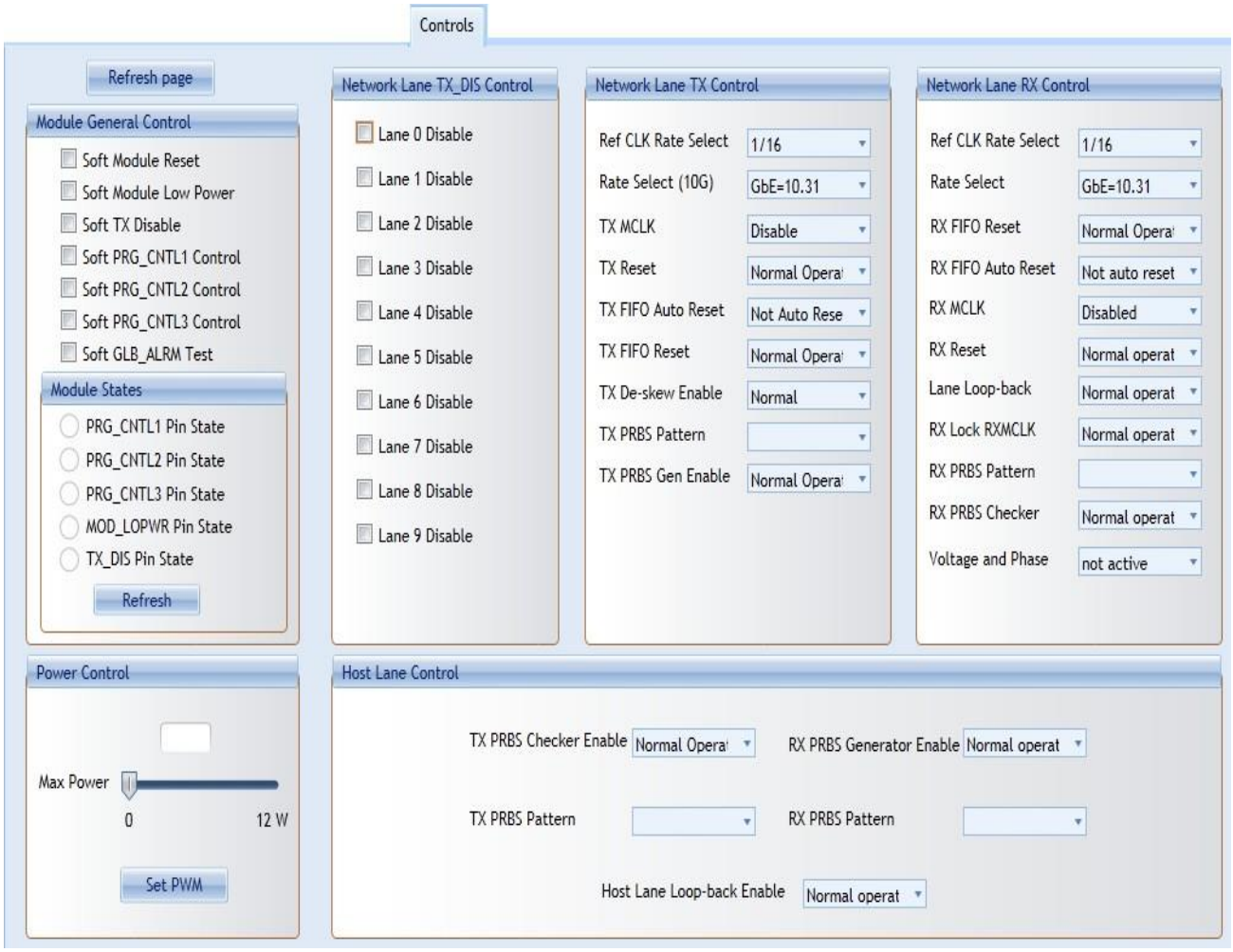


Figure 35 Controls Screen

The control screen shown above in Figure 24 provides additional and alternative controls to hardware pins and programmable control pins in controlling the CFP2 module. Please refer to the CFP MSA memory map for an additional description for each control function below.

I - Module General Control

A010	1			Module General Control	
		RW/SC	15	Soft Module Reset	Register bit for module reset function. Internally, the bit is OR'ed with MOD_RSTn pin. Host write of 0 has no effect. 1: Module reset asserted.
		RW	14	Soft Module Low Power	Register bit for module low power function. OR'ed with MOD_LOPWR pin. 1: Asserted.
		RW	13	Soft TX Disable	Register bit for TX Disable function. OR'ed with TX_DIS pin. 1: Asserted.
		RW	12	Soft PRG_CNTL3 Control	Register bit for PRG_CNTL3 control function. OR'ed with PRG_CNTL3 pin. 1: Asserted.
		RW	11	Soft PRG_CNTL2 Control	Register bit for PRG_CNTL2 control function. OR'ed with PRG_CNTL2 pin. 1: Asserted.
		RW	10	Soft PRG_CNTL1 Control	Register bit for PRG_CNTL1 control function. OR'ed with PRG_CNTL1 pin. 1: Asserted.
		RW	9	Soft GLB_ALRM Test	Command bit for software forced test signal. When this bit is asserted it generates GLB_ALRM signal. 1: Asserted
		RO	8~6	Reserved	
		RO	5	TX_DIS Pin State	Logical state of the TX_DIS pin. 1: Asserted
		RO	4	MOD_LOPWR Pin State	Logical state of the MOD_LOPWR pin. 1: Asserted
		RO	3	PRG_CNTL3 Pin State	Logical state of the PRG_CNTL3 pin. 1: Asserted
		RO	2	PRG_CNTL2 Pin State	Logical state of the PRG_CNTL2 pin. 1: Asserted
		RO	1	PRG_CNTL1 Pin State	Logical state of the PRG_CNTL1 pin. 1: Asserted
		RO	0	Reserved	

Figure 36 CFP MSA Module General Control Register A010

II- Power Control (ML4030 specific)

The user can specify the maximum power consumed by the CFP2 module.

user should adjust Max Power to the desired value, then press Set PWM to set the maximum allowed values for each thermal spot.

III - Thermal Control (ML4030 specific)

Spotted thermal control allows one to control the hot spots in the modules. There are a heating area inside the module which the user can program.

IV- Network Lane n TX_DIS Control

A013	1	RW		Individual Network Lane TX_DIS Control	This register acts upon individual network lanes.
			15	Lane 15 Disable	0: Normal 1: Disable
			14	Lane 14 Disable	0: Normal 1: Disable
			13	Lane 13 Disable	0: Normal 1: Disable
			12	Lane 12 Disable	0: Normal 1: Disable
			11	Lane 11 Disable	0: Normal 1: Disable
			10	Lane 10 Disable	0: Normal 1: Disable
			9	Lane 9 Disable	0: Normal 1: Disable
			8	Lane 8 Disable	0: Normal 1: Disable
			7	Lane 7 Disable	0: Normal 1: Disable
			6	Lane 6 Disable	0: Normal 1: Disable
			5	Lane 5 Disable	0: Normal 1: Disable
			4	Lane 4 Disable	0: Normal 1: Disable
			3	Lane 3 Disable	0: Normal 1: Disable
			2	Lane 2 Disable	0: Normal 1: Disable
			1	Lane 1 Disable	0: Normal 1: Disable
			0	Lane 0 Disable	0: Normal 1: Disable

Figure 37 CFP MSA Individual Network Lane TX_DIS Control Register

V - All Network Lanes TX Control

A011	1			Network Lane TX Control	This control acts upon all the network lanes.	0200h
		RO	15	Reserved		0
		RW	14	TX PRBS Generator Enable	0: Normal operation, 1: PRBS mode. (Optional)	0
		RW	13	TX PRBS Pattern 1	00b:2^7, 01b:2^15, 10b:2^23, 11b:2^31.	00b
		RW	12	TX PRBS Pattern 0		
		RW	11	TX De-skew Enable	0:Normal, 1:Disable	0
		RW	10	TX FIFO Reset	This bit affects both host and network side TX FIFOs. 0: Normal operation, 1: Reset (Optional).	0
		RW	9	TX FIFO Auto Reset	This bit affects both host and network side TX FIFOs. 0: Not Auto Reset, 1: Auto Reset. (Optional).	1
		RW	8	TX Reset	0: Normal operation, 1: Reset. Definition and implementation are vendor specific.	0
		RW	7~5	TX MCLK Control	000b: Disabled, 001b: Reserved, 010b: 1/8 of network lane rate, 011b: Reserved, 100b: 1/64 of network lane rate, 101b: 1/64 of host lane rate, 110b: 1/16 of network lane rate, 111b: 1/16 of host lane rate.	000b
		RO	4	Reserved		0b
		RW	3~1	TX Rate Select (10G lane rate)	000b: GbE=10.31, 001b:SDH=9.95, 010b:OTU3=10.7, 011b:OTU4=11.2, 100b~111b: Reserved.	000b
		RW	0	TX Reference CLK Rate Select	0: 1/16, 1: 1/64.	0b

Figure 38 CFP MSA Network Lane TX Control Register

VI - All Network Lanes RX Control

A012	**1**			**Network Lane RX Control**	**This control acts upon all the network lanes.**	**0200h**
		RW	15	Active Decision Voltage and Phase function	This bit activates the active decision voltage and phase function in the module. 0: not active, 1: active. (Optional)	0b
		RW	14	RX PRBS Checker Enable	0: Normal operation, 1: PRBS mode. (Optional)	0b
		RW	13	RX PRBS Pattern 1	00b: 2^7, 01b: 2^15, 10b: 2^23, 11b: 2^31.	00b
		RW	12	RX PRBS Pattern 0		
		RW	11	RX Lock RX_MCLK to Reference CLK	0: Normal operation, 1: Lock RX_MCLK to REFCLK.	0b
		RW	10	Network Lane Loop-back	0: Normal operation, 1: Network lane loop-back. (Optional)	0b
		RW	9	RX FIFO Auto Reset	0: Not auto reset, 1: Auto reset. (Optional).	1b
		RW	8	RX Reset	0: Normal operation, 1: Reset. Definition and implementation are vendor specific.	0b
		RW	7~5	RX MCLK Control	000b: Disabled, 001b: Reserved, 010b: 1/8 of network lane rate, 011b: Reserved, 100b: 1/64 of network lane rate, 101b: 1/64 of host lane rate, 110b: 1/16 of network lane rate, 111b: 1/16 of host lane rate.	000b
		RW	4	RX FIFO Reset	0: Normal, 1: Reset. (Optional).	0b
		RW	3~1	RX Rate Select	000b: GbE=10.31, 001b:SDH=9.95, 010b:OTU3=10.7, 011b:OTU4=11.2, 100b~111b: Reserved.	000b
		RW	0	RX Reference CLK Rate Select	0: 1/16, 1: 1/64.	0b

Figure 39 CFP MSA Network Lane RX Control Register

VII - Host Lane Control

A014	**1**			**Host Lane Control**	**This control acts upon all the network lanes.**
		RO	15	Reserved	
		RW	14	TX PRBS Checker Enable	0:Normal operation, 1:PRBS mode. (Optional)
		RW	13	TX PRBS Pattern 1	00:2^7, 01:2^15, 10:2^23, 11:2^31
		RW	12	TX PRBS Pattern 0	
		RO	11	Reserved	
		RW	10	Host Lane Loop-back Enable	0: Normal operation, 1: Host lane loop-back. (Optional)
		RO	9~8	Reserved	
		RW	7	RX PRBS Generator Enable	0:Normal operation, 1:PRBS mode. (Optional)
		RW	6	RX PRBS Pattern 1	00b: 2^7, 01b: 2^15, 10b: 2^23, 11b: 2^31
		RW	5	RX PRBS Pattern 0	
		RO	4~0	Reserved	

Figure 40. CFP MSA Host Lane Control

8.6.6 Identification

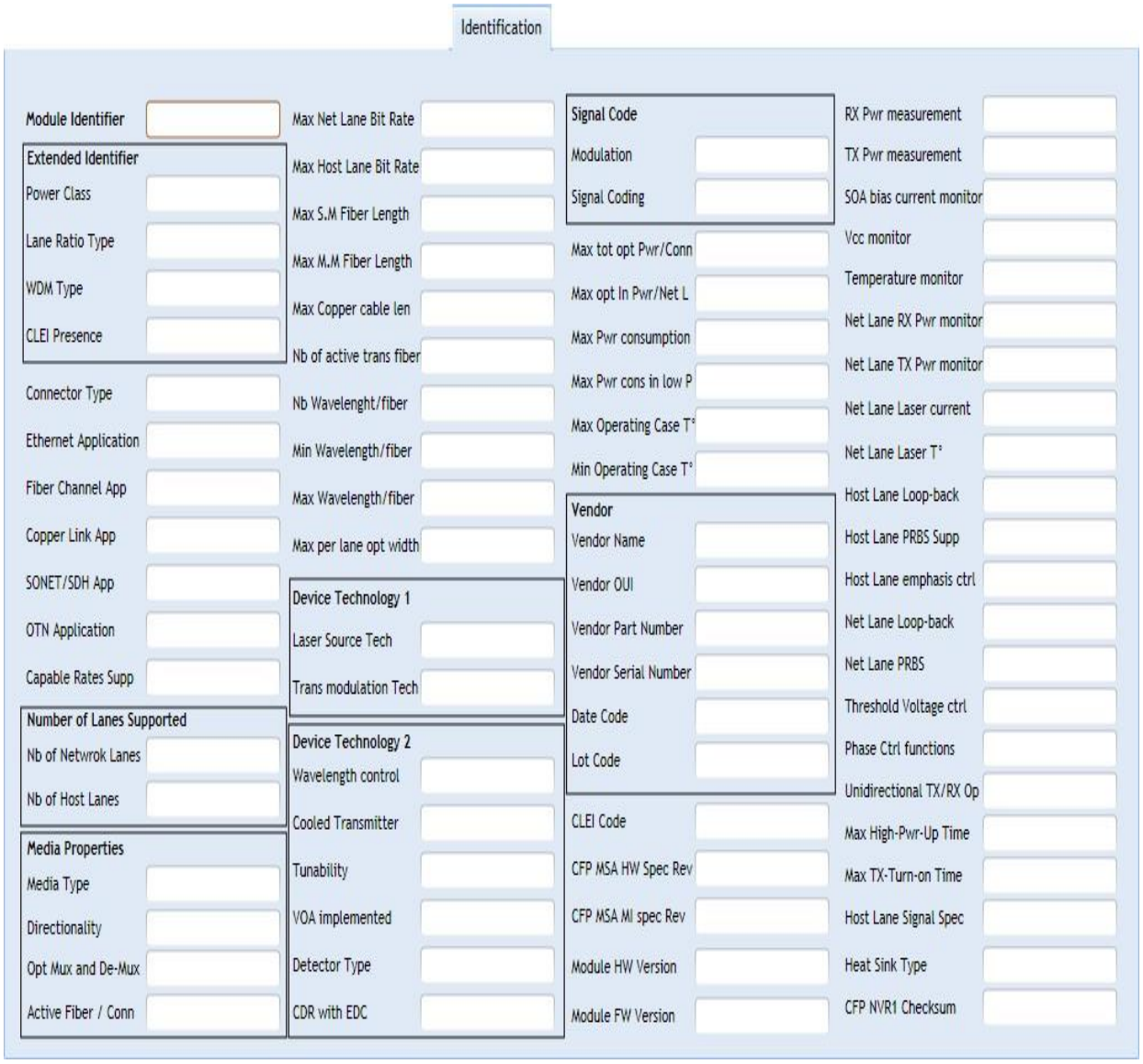


Figure 41 Identification screen

The following sections refers to CFP MSA 1.4 R5 Release, and are presented without any modification or change, the targeted information is read from the correspondent registers, calculated or enumerated when required, and presented to the user on the above screen in a simple readable ASCII format.

8.6.6.1 Module Identifier (8000h)

For CFP MSA compliant modules, this value shall be 0Eh. Other module form factors used in the industry are identified with other values. For details, please refer to CFP NVR Table 1.

8.6.6.2 Extended Identifier (8001h)

It provides additional information about CFP module.

7.3.6.2.1 Power Class

As outlined in the CFP MSA Hardware Specification, there are four power classes identified for the CFP MSA. The power classes are provided to allow the host to identify the power requirements of the module and determine if the system is capable of providing and dissipating the specified power class. For a more detailed description, please refer to the CFP MSA Hardware Specification.

7.3.6.2.2 Lane Ratio Type

The CFP module shall support network interfaces which may comply with various physical interfaces such as IEEE PMD, SONET/SDH, OTN or that from other standards body. For example, 100GBASE-LR4 network interface corresponds to the optical PMD specified in IEEE clause 88. The CFP module shall also support the Host interface which is instantiated as an electrical interface with multiple lanes operating at a nominal 10Gbps.

7.3.6.2.3 WDM Type

It shall identify any optical grid spacing which is in use by the CFP module.

8.6.6.3 Connector Type Code (8002h)

It shall identify the connector technology used for the network interface. Early iterations of the CFP MSA have identified SC optical connectors, and it is expected that further
connectors will be identified.

8.6.6.4 Ethernet Application Code (8003h)

It shall identify what if any Ethernet PMD application is supported. Any CFP module which supports an application not including Ethernet such as SONET/SDH, OTN, Fiber Channel or other, shall record a 00h to signify that the Ethernet application is undefined. Any CFP module which supports an application which includes Ethernet and additional applications such as SONET/SDH, OTN, Fiber Channel or other, shall record the value in Ethernet Application Code corresponding to the supported Ethernet application.

8.6.6.5 Fiber Channel Application Code (8004h)

It shall identify what if any Fiber Channel PMD application is supported. Any CFP module which supports an application not including Fiber Channel such as SONET/SDH, OTN,Ethernet or other, shall record a 00h to signify that the Fiber Channel application is undefined. Any CFP module which supports an application which includes Fiber Channel and additional applications such as SONET/SDH, OTN, Ethernet or other, shall record the value in Fiber Channel Application Code corresponding to the supported Fiber Channel application.

8.6.6.6 Copper Link Application Code (8005h)

In this CFP register, the CFP module shall identify what if any non-Ethernet Copper based PMD application which is supported. At the time of the writing, this application is undefined.

8.6.6.7 SONET/SDH Application Code (8006h)

It shall identify what if any SONET/SDH PMD application is supported. Any CFP module which supports an application not including SONET/SDH such as Ethernet, OTN, Fiber Channel or other, shall record a 00h to signify that the SONET/SDH application is undefined. Any CFP module which supports an application which includes SONET/SDH and additional applications such as Ethernet, OTN, Fiber Channel or other, shall record the value in SONET/SDH Application Code corresponding to the supported SONET/SDH application.

8.6.6.8 OTN Application Code (8007h)

It shall identify what if any OTN PMD application is supported. Any CFP module which supports an application not including OTN such as SONET/SDH, Ethernet, Fiber Channel or other, shall record a 00h to signify that the OTN application is undefined. Any CFP module which supports an application which includes OTN and additional applications such as SONET/SDH, Ethernet, Fiber Channel or other, shall record the value in OTN Application Code corresponding to the supported OTN application.

8.6.6.9 Additional Capable Rates Supported (8008h)

8.6.6.10 Number of Lanes Supported (8009h)

The network lane number assignment shall always start from 0h and end with the number of lanes supported minus one, with no number skipped in between. This shall be applicable to both network and host lanes whether the lane numbers are different or the same. For example, a serial network lane implementation shall use lane 0 and a 4 network lane PMD shall use lane number 0 ~ 3. A CAUI host interface shall use lane numbers 0 ~ 9.

7.3.6.2.4 Number of Network Lanes

It is a 4-bit number representing the number of network data I/O supported in this module. The value of 0 represents 16 network data I/O supported. The values of 1 through 15 represent the actual number of network lanes supported.

7.3.6.2.5 Number of Host Lanes

It is a 4-bit number representing the number of host data I/O supported in this module. The value of 0 represents 16 host data I/O supported. The values of 1 through 15 represent the actual number of host lanes supported.

8.6.6.11 Media Properties (800Ah)

7.3.6.2.6 Media Type

It shall identify the type of transmission media for the supported application using bits 7~6.

7.3.6.2.7 Directionality

It shall identify if supported application uses the same transmission media for the transmit/receive network interfaces (Bi-Directional) or if separate transmission media are required for transmit and receive network interfaces, respectively.

7.3.6.2.8 Optical Multiplexing and De-Multiplexing

It shall identify if optical multiplexing and optical de-multiplexing are supported within the CFP module.

7.3.6.2.9 Active Fiber per Connector

It shall identify the number of active TX/RX fiber pairs in an optical connector. For

example, a CFP module supporting the 100GBASE-SR10 application using an MPO connector shall report 10 in Active Fiber per Connector.

8.6.6.12 Maximum Network Lane Bit Rate (800Bh)

It shall identify maximum data rate supported per network lane. For more complex modulation schemes than OOK (on/off keying), the value reported shall be the bit rate and not the baud rate. The value shall be based upon units of 0.2 Gbps. A value of 0h is considered undefined.

8.6.6.13 Maximum Host Lane Bit Rate (800Ch)

It shall identify maximum data rate supported per host lane. The value shall be based upon units of 0.2 Gbps. The nominal lane rate suggested in the CFP MSA HW Specification is 10Gbps. However, various applications such as support for OTU4 and future applications will require higher lane rates. A value 0h is considered undefined.

8.6.6.14 Maximum Single Mode Optical Fiber Length (800Dh)

It shall identify the specified maximum reach supported by the application for transmission over single mode fiber. The value shall be based upon units of 1km. For applications which operate over compensated transmission systems, it is suggested to enter an undefined value. A value of 0h is considered undefined.

8.6.6.15 Maximum Multi-Mode Optical Fiber Length (800Eh)

It shall identify the specified maximum reach supported by the application for transmission over OM3 multi-mode fiber. The value shall be based upon units of 10 m. A value of 0h is considered undefined.

8.6.6.16 Maximum Copper Cable Length (800Fh)

The module shall identify the specified maximum reach supported by the application for transmission over copper cable. The value shall be based upon units of 1 m. A value of 0h is considered undefined.

8.6.6.17 Transmitter Spectral Characteristics 1 (8010h)

7.3.6.2.10 Number of Active Transmit Fibers

Bits 4~0 are a value identifying the number of active optical fiber outputs supported. The value 0 represents 0 active transmit fibers (i. e., receive-only), copper or undefined. The values of 1 through 31 represent the actual number of active transmit fibers. For example, the value for 100GBASE-SR10 is 10.

8.6.6.18 Transmitter Spectral Characteristics 2 (8011h)

7.3.6.2.11 Number of Wavelengths per Active Transmit Fiber

Bits 4~0 are a value representing the number of wavelengths per active transmit fiber. The value 0h represents an 850 nm multimode source or undefined. The values 1 through 31 represent the actual number of wavelengths per transmit fiber. For example, the value for 100GBASE-LR4 is 4.

8.6.6.19 Minimum Wavelength per Active Fiber (8012h, 8013h)

It is a 16-bit unsigned value data field and shall identify the minimum wavelength, in the unit of 25 pm, of any supported optical fiber output per the application. For an example, the value for 100GBASE-LR4 with a minimum specified wavelength of 1294.53 nm would be CA45h. A value of 0 indicates a multimode source or undefined.

8.6.6.20 Maximum Wavelength per Active Fiber (8014h, 8015h)

It is a 16-bit unsigned value data field and shall identify the maximum wavelength, in the unit of 25 pm, of any supported optical fiber output per the application. For an example, the value for 100GBASE-LR4 with

a maximum specified wavelength of 1310.19 nm would be CCB8h. A value of 0 indicates a multimode source or undefined.

8.6.6.21 Maximum per Lane Optical Width (8016h, 8017h)

It shall identify the maximum network lane optical wavelength width, in the unit of 1pm, of any supported optical fiber output per the application. For an example, the value for
100GBASE-LR4 with a maximum specified optical wavelength width of 2.1nm for network lane L3 would be 834h. A value of 0 indicates a multimode source or undefined.

8.6.6.22 Device Technology 1 (8018h)

7.3.6.2.12 Laser Source Technology

It shall identify the type of laser technology which is used. There is a CFP register value for electrical/copper (non-laser) transmission, as well as additional reserved space for as of yet undefined laser types.

7.3.6.2.13 Transmitter Modulation Technology

It shall identify the type of modulation technology used. This is a 4-bit unsigned value
representing commonly used modulation technologies with reserved values to represent for as of yet undefined modulator types.

8.6.6.23 Device Technology 2 (8019h)

Several data fields in this register are related to tunable transmitters. However the full
support of tunability is not fully covered in the Draft. It shall be supported either in the future release of this draft or in a follow-up MSA.

7.3.6.2.14 Wavelength Control

It shall identify if the wavelength of the laser technology which is used includes an active wavelength control mechanism. Active wavelength control mechanism is defined to be a wavelength sensitive device which can be used to compare the actual transmitted wavelength from the expected transmitted wavelength. The value of 0b signifies no control mechanism and 1b signifies the presence of such a mechanism within the CFP module.

7.3.6.2.15 Cooled Transmitter

It shall identify if the transmitter is coupled to a cooling mechanism within the module. A
popular implementation for such a coupled cooling mechanism is to mount a laser such that it is thermally coupled to a thermoelectric cooler which is controlled to keep the laser within a defined temperature range. If any cooling mechanism is present the transmitter is considered to be cooled. A transmitter is considered to be cooled even if the cooling mechanism is not always active. The value of 0b signifies no cooling mechanism and 1b signifies the presence of such a cooling mechanism within the CFP module.

7.3.6.2.16 Tunability

It shall identify if the transmitted optical wavelength may be tuned over a specified spectral range. The value of 0b signifies no tuning mechanism and 1b signifies the presence of such a tuning mechanism within the CFP module.

7.3.6.2.17 VOA Implemented

It shall identify if the optical receiver implements a variable optical attenuator (VOA) within the optical receive chain. The value of 0b signifies no VOA mechanism and 1b signifies the presence of such a VOA mechanism within the CFP module.

7.3.6.2.18 Detector Type

It shall identify the type of detector technology which is used. There is a CFP register value for undefined detector types.

7.3.6.2.19 CDR with EDC

It shall identify if the Clock and Data Recovery (CDR) circuitry within the CFP module receive path contains any electronic dispersion compensation (EDC) techniques to improve the receiver performance. It is recognized that there exist a variety of EDC techniques with varying performance enhancements and tradeoffs – this CFP register does not convey any detail, only if the CFP module implements EDC within the receiver. The value of 0b signifies no EDC mechanism and "1" signifies the presence of such an EDC mechanism within the CFP module.

8.6.6.24 Signal Code (801Ah)

7.3.6.2.20 Modulation

It shall identify the polarity coding used in the optical modulation. A value of 0b is considered undefined.

7.3.6.2.21 Signal Coding

It shall identify the signaling coding used in the optical modulation. A value of 0b is considered undefined.

8.6.6.25 Maximum Total Optical Output Power per Connector (801Bh)

It shall identify the maximum optical output power of any supported optical fiber output per the application. A value of 0h is considered undefined.

8.6.6.26 Maximum Optical Input Power per Network Lane (801Ch)

It shall identify the maximum optical input power of any supported optical fiber input per the application. A value of 0h is considered undefined.

8.6.6.27 Maximum Power Consumption (801Dh)

It shall identify the maximum power consumption of any supported application. A value of 0h is considered undefined.

8.6.6.28 Maximum Power Consumption in Low Power Mode (801Eh)

It shall identify the maximum power consumption of the low power mode state. The low power mode state is described in detail in the CFP MSA Hardware specification. A value of 0h is considered undefined.

8.6.6.29 Maximum Operating Case Temp Range (801Fh)

It shall identify the maximum operating case temperature specified of any supported application. It is a signed 8-bit value expressed in two's-complement, representing a total range from -127 to +127 in increments of 1 degree C'. The value -128 (80h) indicates the value is not defined.

8.6.6.30 Minimum Operating Case Temp Range (8020h)

It shall identify the minimum operating case temperature specified of any supported application. It is a signed 8-bit value expressed in two's-complement, representing a total range from -127 to +127 in increments of 1 degree C'. The value -128 (80h) indicates the value is not defined.

8.6.6.31 Vendor Name (8021h)

It shall identify the CFP module Vendor name in ASCII code. The vendor name is a 16 byte field that contains ASCII characters, left aligned and padded on the right with ASCII spaces (20h). The vendor name shall be the full name of the corporation, a commonly accepted abbreviation of the name or the stock exchange code for the corporation. Vendor is the CFP module vendor.

8.6.6.32 Vendor OUI (8031h)

It is a 3 byte field that contains the IEEE Company Identifier for CFP module vendor (as opposed to the OUI of any third party ICs which may be used therein). Bit order for the OUI follows the format of IEEE 802.3 Clause 22.2.4.3.1 and is therefore reversed in comparison to other NVRs. A value of all zero in the 3 byte field indicates that the Vendor OUI is unspecified. Vendor is the CFP module vendor.

8.6.6.33 Vendor Part Number (8034h)

It is a 16 byte field that contains ASCII characters, left aligned and padded on the right with ASCII spaces (20h), defining the vendor part number or product name. A value of all zero in the 16 byte field indicates that the Vendor Part Number is unspecified. Vendor is the CFP module vendor.

8.6.6.34 Vendor Serial Number (8044h)

It is a 16 byte field that contains ASCII characters, left aligned and padded on the right with ASCII spaces (20h), defining the vendor's serial number. A value of all zero in the 16 byte field indicates that the Vendor SN is unspecified. Vendor is the CFP module vendor.

8.6.6.35 Date Code (8054h)

It is an 8 byte field that contains the vendor's date code in ASCII characters. A value of all zero in the 8 byte field indicates that the Vendor date code is unspecified. Vendor is the CFP module vendor.

8.6.6.36 Lot Code (805Ch)

It is a 2-byte field that contains the vendor's lot code in ASCII characters. A value of all zero in the 2-byte field indicates that the Vendor lot code is unspecified. Vendor is the CFP module vendor.

8.6.6.37 CLEI Code (805Eh)

It is a 10 byte field that contains the Common Language Equipment Identifier code in ASCII characters. A value of all zero in the 10 byte field indicates that the CLEI code is unspecified.

8.6.6.38 CFP MSA Hardware Specification Revision Number (8068h)

It indicates the CFP MSA hardware specification version number supported by the transceiver. This 8-bit value represents the version number times 10. This yields a max of 25.5 revisions.

8.6.6.39 CFP MSA Management Interface Specification Revision Number (8069h)

It indicates the CFP MSA Management specification version number supported by the CFP module. This 8-bit value represents the version number times 10. This yields a max of 25.5 revisions.

8.6.6.40 Module Hardware Version Number (806Ah)

It is a 2-byte number in the format of x.y with x at lower address and y at higher address. In each register this 8-bit value represents the version number from 0 to 255. A value of all zero in this 2-byte field indicates that the vendor HW version number is unspecified.

8.6.6.41 Module Firmware Version Number (806Ch)

It is a 2-byte field in the format of "x.y". The "x" value is contained within the lower address. The "y" value is contained in the upper address. In each register this 8-bit value represents the release number from 0 to 255. A value of all zero in this 2-byte field indicates that the vendor FW version number is unspecified.

8.6.6.42 Digital Diagnostic Monitoring Type (806Eh)

It is a one byte field with 8 single bit indicators describing how DDM functions are implemented in CFP module.

8.6.6.43 Digital Diagnostic Monitoring Capability 1 (806Fh)

It describes DDM functions implemented at CFP module level (not lane specific). This MSA draft specifies 4 A/D inputs, transceiver SOA bias current monitor, transceiver power supply voltage monitor, transceiver internal temperature monitor, and transceiver case temperature monitor. The last quantity, transceiver case temperature monitor is intended for supplying an additional monitor to transceiver internal temperature monitor. The definition and implementation of case temperature is left to be specified by vendor datasheet.

8.6.6.44 Digital Diagnostic Monitoring Capability 2 (8070h)

It describes DDM functions implemented at network lane level.

8.6.6.45 Module Enhanced Options (8071h)

It describes enhanced optional functions implemented in CFP module. Refer to register description for details.

8.6.6.46 Maximum High-Power-up Time (8072h)

It is for a vendor defined parameter which specifies the maximum time to transit the "High- Power-up" state shown in *Figure 3 State Transition Diagram during Startup and Turn-off*. The Host may use this value as the time-out value. It is an unsigned 8-bit value * 1 second. Use 1 second if the actual time is less than one second.

8.6.6.47 Maximum TX-Turn-on Time (8073h)

It is for a vendor defined parameter which specifies the maximum time to transit the "TX Turn-on" state shown in *Figure 3 State Transition Diagram during Startup and Turn-off*. The Host may use this value as the time-out value. It is an unsigned 8-bit value in units of 1 second. Use 1 second if the actual time is less than 1 second.

8.6.6.48 Host Lane Signal Spec (8074h)

It specifies the host lane signal type a module supports. Refer to register description for details.

8.6.6.49 Heat Sink Type (8075h)

It identifies if the top surface of the CFP module has a flat top or integrated heat sink. The CFP MSA supports various networking applications which may require different thermal management solutions. The default top surface of the CFP module is a flat top, however, some networking applications will benefit from an integrated heat sink. An integrated heat sink complies with the total module height requirements and shall not disrupt, disable nor damage any riding heat sink system. For further details, refer to the CFP MSA Hardware specification.

8.6.6.50 Maximum TX-Turn-off Time (8076h)

It is for a vendor defined parameter which specifies the maximum time to transit the "TX Turn-off" state shown in *Figure 3 State Transition Diagram during Startup and Turn-off*. The Host may use this value as the time-out value. It is an unsigned 8-bit value in units of ms. Use 1 ms if the actual time is less than 1 second.

8.6.6.51 Maximum High-Power-down Time (8077h)

It is for a vendor defined parameter which specifies the maximum time to transit the "High- Power-down" state shown in *Figure 3 State Transition Diagram during Startup and Turn-off*. The Host may use this value as the time-out value. It is an unsigned 8-bit value * 1 second. Use 1 second if the actual time is less than one second.

8.6.6.52 Module Enhanced Options 2 (8078h)

It describes the second enhanced optional functions implemented in CFP module. Refer to register description for details.

8.6.6.53 Transmitter Monitor Clock Options (8079h)

This register contains the transmitter monitor clock option bits. The clock is intended to be used as a reference for measurements of the optical output. If provided, the clock shall operate at a rate relative to the optical lane rate of 1/16 rate for 40Gbit/s applications and a 1/8 rate of 25Gbit/s for 100Gbit/s applications. Another option is a clock at 1/16 or 1/64 the rate of transmitter electrical input data.

8.6.6.54 Receiver Monitor Clock Options (807Ah)

This register contains the receiver monitor clock option bits. The clock is intended to be used as a reference for measurements of the optical input. If provided, the clock shall operate at a rate relative to the optical lane rate of 1/16 rate for 40Gbit/s applications and a 1/8 rate of 25Gbit/s for 100Gbit/s applications. Another option is a clock at 1/16 or 1/64 the rate of transmitter electrical input data.

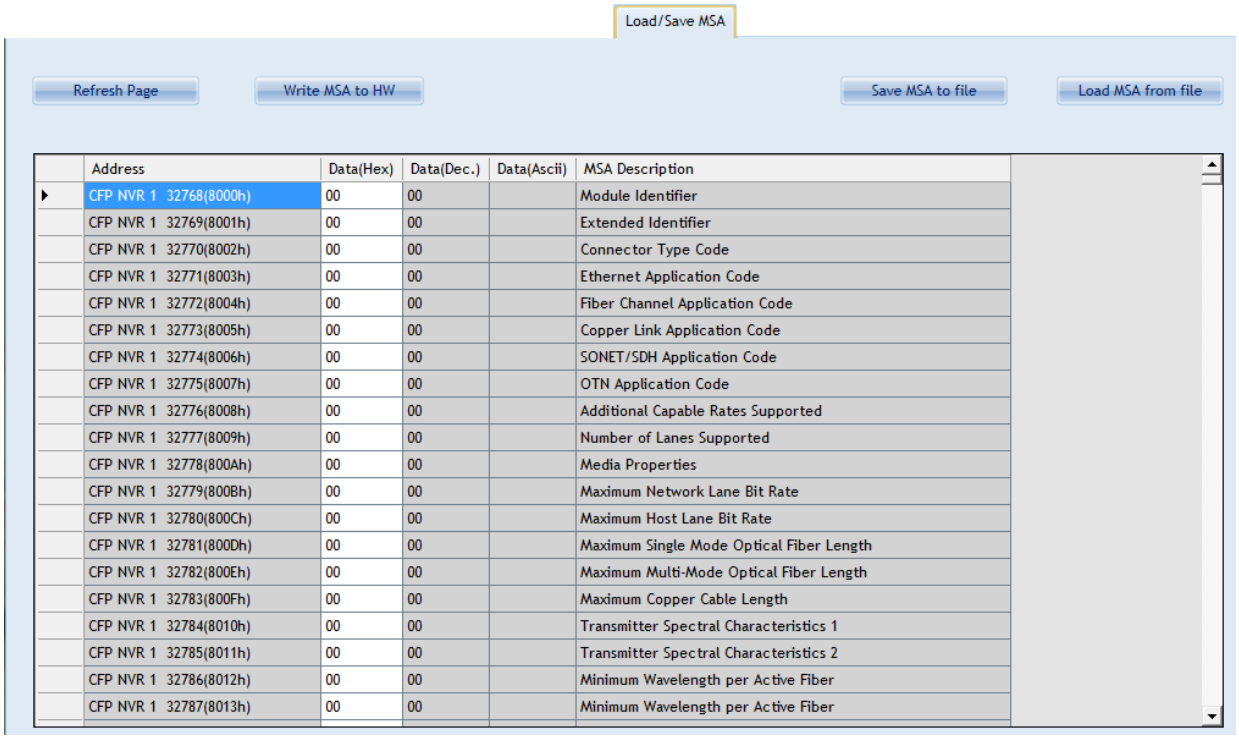
8.6.6.55 Module Enhanced Options 3 (807Bh)

It describes the third enhanced optional functions implemented in CFP module. Refer to register description for details.

8.6.6.56 CFP NVR 1 Checksum (807Fh)

It is the 8 bit unsigned result of the checksum of all of the CFP register LSB contents from addresses 8000h to 807Eh inclusive. Note that all the reserved registers have zero value contribution to the calculation of this Checksum.

8.6.7 Load/Save MSA



Address	Data(Hex)	Data(Dec.)	Data(Ascii)	MSA Description
CFP NVR 1 32768(8000h)	00	00		Module Identifier
CFP NVR 1 32769(8001h)	00	00		Extended Identifier
CFP NVR 1 32770(8002h)	00	00		Connector Type Code
CFP NVR 1 32771(8003h)	00	00		Ethernet Application Code
CFP NVR 1 32772(8004h)	00	00		Fiber Channel Application Code
CFP NVR 1 32773(8005h)	00	00		Copper Link Application Code
CFP NVR 1 32774(8006h)	00	00		SONET/SDH Application Code
CFP NVR 1 32775(8007h)	00	00		OTN Application Code
CFP NVR 1 32776(8008h)	00	00		Additional Capable Rates Supported
CFP NVR 1 32777(8009h)	00	00		Number of Lanes Supported
CFP NVR 1 32778(800Ah)	00	00		Media Properties
CFP NVR 1 32779(800Bh)	00	00		Maximum Network Lane Bit Rate
CFP NVR 1 32780(800Ch)	00	00		Maximum Host Lane Bit Rate
CFP NVR 1 32781(800Dh)	00	00		Maximum Single Mode Optical Fiber Length
CFP NVR 1 32782(800Eh)	00	00		Maximum Multi-Mode Optical Fiber Length
CFP NVR 1 32783(800Fh)	00	00		Maximum Copper Cable Length
CFP NVR 1 32784(8010h)	00	00		Transmitter Spectral Characteristics 1
CFP NVR 1 32785(8011h)	00	00		Transmitter Spectral Characteristics 2
CFP NVR 1 32786(8012h)	00	00		Minimum Wavelength per Active Fiber
CFP NVR 1 32787(8013h)	00	00		Minimum Wavelength per Active Fiber

Figure 42 Load/Save MSA screen

this screen allows user to Load or Save his custom CFP2 configuration .
once data is gathered , it will be displayed in a grid showing : register address, hex value, ASCII value, register description.

- **Refresh Page button:** Read CFP MSA Registers, and refresh values.
- **Write MSA to HW button:** Write the current MSA configuration to CFP2 module.
- **Save MSA to file button:** saves the current MSA memory to a file using csv(comma separated values) format.
- **Load MSA from file button:** Loads MSA values from file and map it to MSA memory.

8.6.8 CFP Module Vendor I/O pins

These pins can be controlled by the external pin header J18 on the Host Board, or from the GUI.

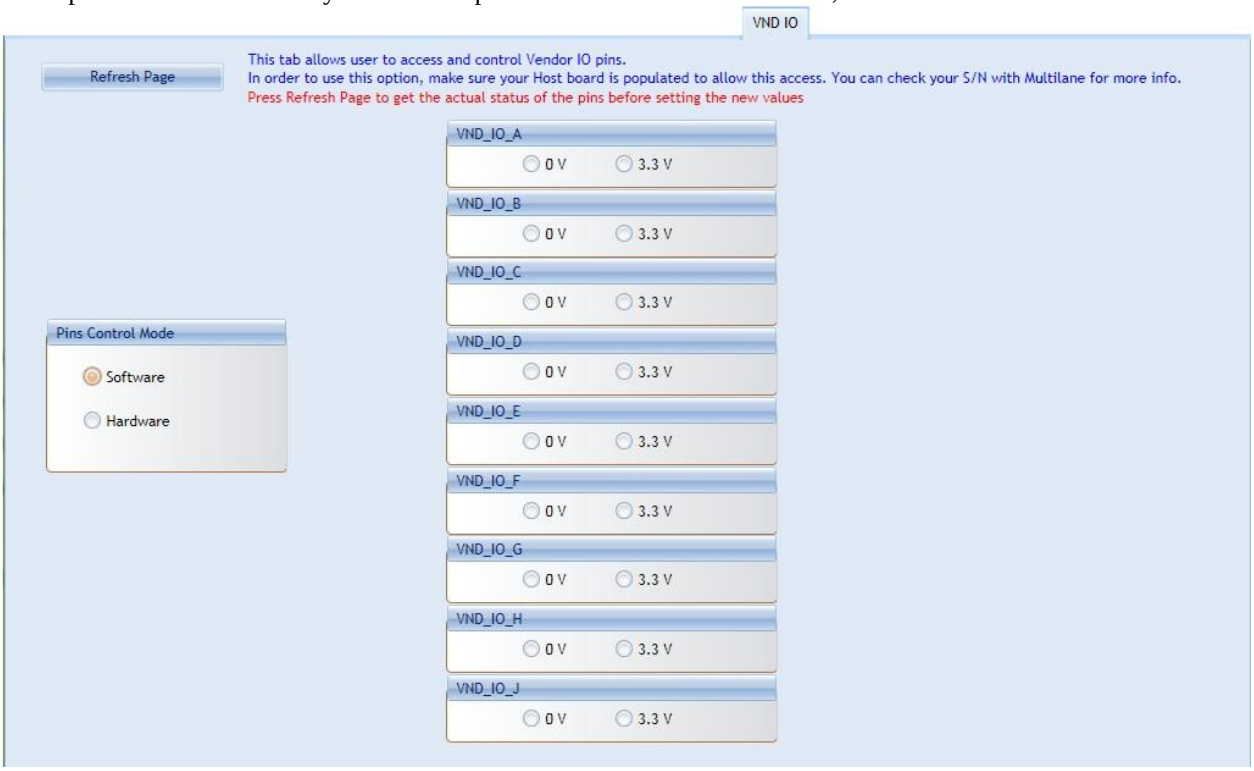


Figure 43. VND IO Tab

This is the VND IO tab which provides control access to CFP2 Module Vendor I/O pins.

In Pins Control Mode

-Select Software option to gain Software control for VND_IO pins, and drive them from the host microcontroller

-Select Hardware option to release the pins from microcontroller and control them from pin header male J18 on the Host by either applying 3.3V or 0V from an external source.

Software Mode:

The Refresh Page button will read the current pins status and update the GUI values accordingly, thus user can check the current state of all VND_IO pins at any time by pressing the refresh button.

Each VND_IO pin can be controlled from its corresponding GroupBox, allowing user to set any pin independently to 0V or 3.3V.

8.6.9 Monitor ACO

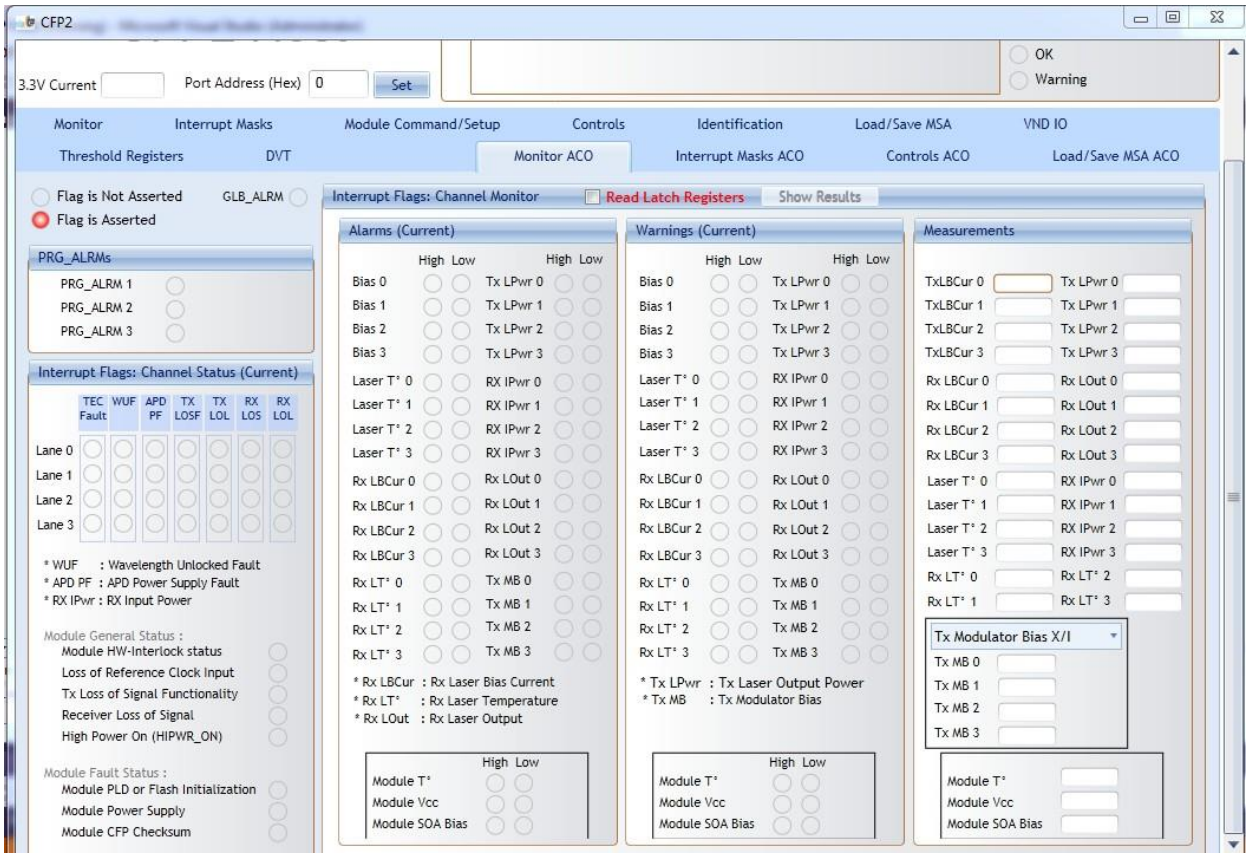


Figure 44. Monitor ACO tab

The Monitor ACO Window shown in Figure 43 above is the main source of the module status and alarm/warning flags conditions. It shows the current status of a flag, the default flag update rate is 2 Hz, so the flag status is updated every 0.5 seconds.

8.6.9.1 Flag Statuses:

- Flag is not asserted: the corresponding LED is OFF (Transparent).
- Flag is asserted: the corresponding LED is ON (Red).

8.6.9.2 Read Latch Registers Option

If the **Read Latch Registers** checkbox is checked, the Show Results button is enabled and it must be clicked so the latched flag statuses are shown. Note that a label will appear indicating the exact time when the results are shown. Then, it is possible to refresh the results by clicking the button again, and the time will be updated according to the latest results shown.

8.6.9.3 PRG_Alarms

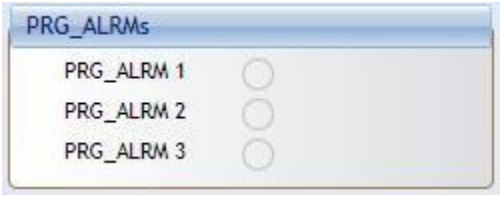


Figure 45. PRG Alarms

PRG_ALRM1, PRG_ALRM2 and PRG_ALRM3 are programmable alarm pins that can be programmed with custom alarm sources. When the custom select alarm is enabled, the corresponding LED is asserted on the monitor screen. Please refer to section 3.3-II for information about how to set a custom alarm source for PRG_ALRMs.

8.6.9.4 Interrupt flags: Channel Status

- **Current**:

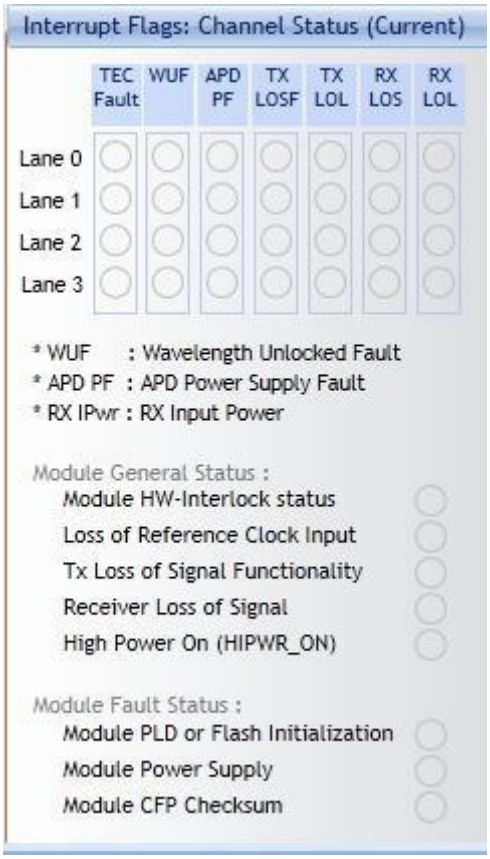


Figure 46. Interrupt flags: Channel Status (Current)

B1A0 [2.0]	16	RO		Network Lane n Fault and Status	16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent.	0000h
			15	Lane TEC Fault	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
			14	Lane Wavelength Unlocked Fault	0: Normal; 1: Asserted. (FAWS_TYPE_C)	0
			13	Lane APD Power Supply Fault	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
			12~8	Reserved		0
			7	Lane TX_LOSF	0: Normal; 1: Asserted. (PMD) (FAWS_TYPE_C)	0
			6	Lane TX_LOL	0: Normal; 1: Asserted. (Network) (FAWS_TYPE_B)	0
			5	Reserved		0
			4	Lane RX_LOS	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
			3	Lane RX_LOL	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
			2	Lane RX FIFO error	0: Normal, 1: Error. (FAWS_TYPE_B)	0
			1	Lane RX TEC Fault	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
			0	Reserved.		0

Figure 47. Network Lane n Fault and Status (current)

B01E [2.0]	1	RO		Module Fault Status	Module Fault Status bit pattern. Only fatal faults that are potentially harmful to the module can trigger the bits here. All the bits are 0: Normal; 1: fault detected. When any bit in this register is a '1', The Module State register will also be set to the Fault State.	0000h
			15	Reserved	Reserved for extension of "other faults" in case of all the bits used up in this register.	0
			14~7	Reserved		0
			6	PLD or Flash Initialization Fault	PLD, CPLD, or FPGA initialization fault. (FAWS_TYPE_A)	0
			5	Power Supply Fault	1: Power supply is out of range. (FAWS_TYPE_A)	0
			4~2	Reserved		000b
			1	CFP Checksum Fault	1: CFP Checksum failed. (FAWS_TYPE_A)	0
			0	Reserved		0

Figure 48. Module Fault Status (current)

B01D [2.0]	1	RO		**Module General Status**		0000h
			15	Reserved		0
			14	Reserved		0
			13	HW_Interlock	Module internally generated status signal. (FAWS_TYPE_A) 0: If module power <= Host cooling capacity or if hardware Interlock is not used, 1: If module power > Host cooling capacity. For non-pluggable modules (e.g. MSA-100GLH module), PRG_CNTL3 pin should be set to "1" during initialization state.	0
			12~11	Reserved		0
			10	Loss of REFCLK Input	Loss of reference clock input. It is an optional feature. (FAWS_TYPE_B). 0: Normal, 1: Loss of signal.	0
			9	TX_JITTER_PLL_LOL	TX jitter PLL loss of lock. It is an optional feature. (FAWS_TYPE_B). 0: Normal, 1: Loss of lock.	0
			8	TX_CMU_LOL	TX CMU loss of lock. It is the loss of lock indicator on the network side of the CMU. It is an optional feature. (FAWS_TYPE_B). 0: Normal, 1: Loss of lock.	0
			7	TX_LOSF	Transmitter Loss of Signal Functionality. Logic OR of all of Network Lanes TX_LOSF bits. PRG_ALRMx mappable. . (FAWS_TYPE_C, since the TX must be enabled). **Note: The corresponding latch register is set to 1 on any change (0-->1 or 1 --> 0) of this status signal.** 0: all transmitter signals functional, 1: any transmitter signal not functional.	0
			6	TX_HOST_LOL	TX IC Lock Indicator. Logic OR of all host lane TX_LOL bits. PRG_ALRMx mappable. (FAWS_TYPE_B). **Note: The corresponding latch register is set to 1 on any change (0-->1 or 1 --> 0) of this status signal.** 0: Locked, 1: Loss of lock.	0
			5	RX_LOS	Receiver Loss of Signal. Logic OR of all of network lane RX_LOS bits. (FAWS_TYPE_B). **Note: The corresponding latch register is set to 1 on any change (0-->1 or 1 --> 0) of this status signal.** 0: No network lane RX_LOS bit asserted, 1: Any network lane RX_LOS bit asserted.	0
			4	RX_NETWORK_LOL	RX IC Lock Indicator. Logic OR of all network lane RX_LOL bits. PRG_ALRMx mappable. (FAWS_TYPE_B). **Note: The corresponding latch register is set to 1 on any change (0-->1 or 1 --> 0) of this status signal.** 0: Locked, 1: Loss of lock.	0
			3	Out of Alignment	Host lane skew out of alignment indicator. Applicable only for some internal implementations. (FAWS_TYPE_B).	0
					0: Normal, 1: Out of alignment.	
			2	Performance Monitor Interval Complete	0: Not Done 1:Done.	0
			1	HIPWR_ON	Status bit representing the condition of module in high power status. FAWS Type is not applicable. 0: Module is not in high power on status, 1: Module is in high powered on status.	0
			0	Reserved		0

Figure 49. CFP MSA Module General Status (current)

- **Latch**:

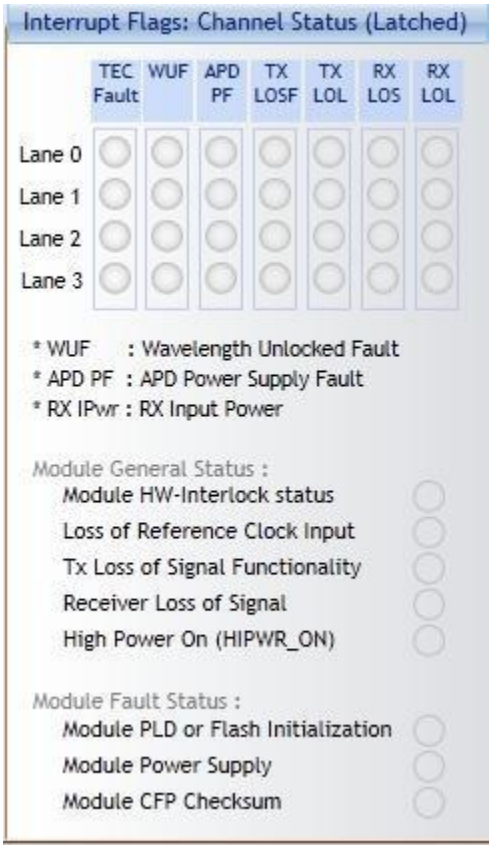


Figure 50. Interrupt flags: Channel Status (Latched)

B1D0 [2.0]	**16**			**Network Lane n Fault and Status Latch**	**16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent.**	**0000h**
		RO/LH/COR	15	Lane TEC Fault Latch	1: Latched.	0
		RO/LH/COR	14	Lane Wavelength Unlocked Fault Latch	1: Latched.	0
		RO/LH/COR	13	Lane APD Power Supply Fault Latch	1: Latched.	0
		RO	12~8	Reserved		0
		RO/LH/COR	7	Lane TX_LOSF Latch	1: Latched.	0
		RO/LH/COR	6	Lane TX_LOL Latch	1: Latched.	0
		RO	5	Reserved		0
		RO/LH/COR	4	Lane RX_LOS Latch	1: Latched.	0
		RO/LH/COR	3	Lane RX_LOL Latch	1: Latched.	0
		RO/LH/COR	2	Lane RX FIFO Status Latch	1: Latched.	0
		RO/LH/COR	1	Lane RX TEC Fault Latch	1: Latched.	0
		RO	0	Reserved		0

Figure 51. Network Lane n Fault and Status Latch

B023 [2.0]	1			**Module General Status Latch**		**0000h**
		RO	15	Reserved		0
		RO	14	Reserved		0
		RO/LH/COR	13	HW_Interlock Latch	1: Latched.	0
		RO	12~11	Reserved		0
		RO/LH/COR	10	Loss of REFCLK Input Latch	1: Latched.	0
		RO/LH/COR	9	TX_JITTER_PLL_LOL Latch	1: Latched.	0
		RO/LH/COR	8	TX_CMU_LOL Latch	1: Latched.	0
		RO/LH/COR	7	TX_LOSF Latch	1: Latched. **Note:** Set to 1 on any change (0-->1 or 1 --> 0) of the corresponding status signal.	0
		RO/LH/COR	6	TX_HOST_LOL Latch	1: Latched. **Note:** Set to 1 on any change (0-->1 or 1 --> 0) of the corresponding status signal.	0
		RO/LH/COR	5	RX_LOS Latch	1: Latched. **Note:** Set to 1 on any change (0-->1 or 1 --> 0) of the corresponding status signal.	0
		RO/LH/COR	4	RX_NETWORK_LOL Latch	1: Latched. **Note:** Set to 1 on any change (0-->1 or 1 --> 0) of the corresponding status signal.	0
		RO/LH/COR	3	Out of Alignment Latch	1: Latched.	0
		RO/LH/COR	2	Performance Monitor Interval Complete Latch	1: Latched.	0
		RO	1~0	Reserved		000b

Figure 52. Module General Status Latch

B024 [2.0]	1			**Module Fault Status Latch**	**Module Fault Status latched bit pattern.**	**0000h**
		RO	15~7	Reserved		0
		RO/LH/COR	6	PLD or Flash Initialization Fault Latch	1: Latched.	0
		RO/LH/COR	5	Power Supply Fault Latch	1: Latched.	0
		RO	4~2	Reserved		000b
		RO/LH/COR	1	CFP Checksum Fault Latch	1: Latched.	0
		RO	0	Reserved		0

Figure 53. Module Fault Status Latch

8.6.9.5 Interrupt Flags: Channel Monitor-Alarms and Warnings

- **Current:**

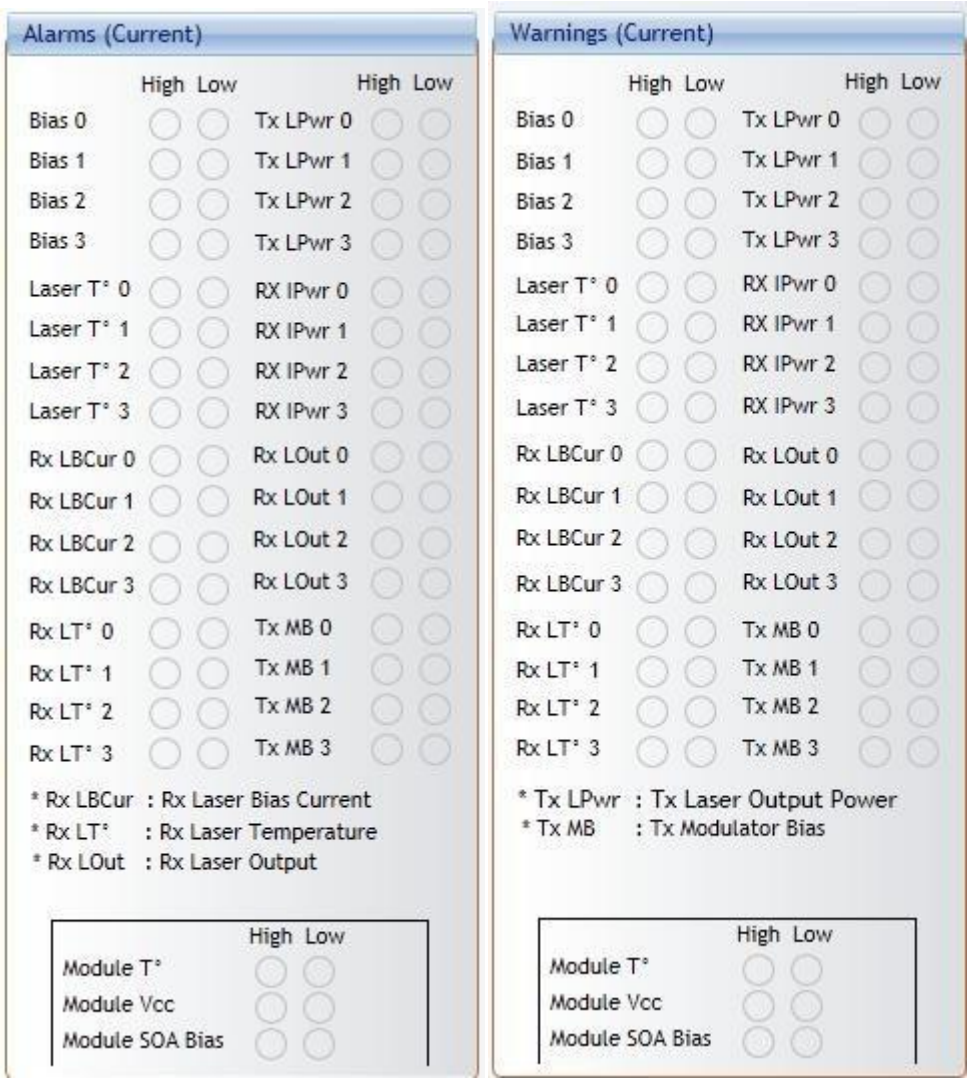


Figure 54. Network Lane n Alarms and Warnings (Current)

Network Lane VR 1						
Hex Addr	*Size*	*Access Type*	*Bit*	*Register Name* *Bit Field Name*	*Description*	*Init Value*
Network Lane FAWS Registers						
B180 [2.0]	**16**	**RO**		**Network Lane n Alarm and Warning 1**	**16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent.**	**0000h**
			15	Bias High Alarm	0: Normal; 1: Asserted. (FAWS_TYPE_C)	0
			14	Bias High Warning	0: Normal; 1: Asserted. (FAWS_TYPE_C)	0
			13	Bias Low Warning	0: Normal; 1: Asserted. (FAWS_TYPE_C)	0
			12	Bias Low Alarm	0: Normal; 1: Asserted. (FAWS_TYPE_C)	0
			11	TX Power High Alarm	0: Normal; 1: Asserted. (FAWS_TYPE_C)	0
			10	TX Power High Warning	0: Normal; 1: Asserted. (FAWS_TYPE_C)	0
			9	TX Power Low Warning	0: Normal; 1: Asserted. (FAWS_TYPE_C)	0
			8	TX Power Low Alarm	0: Normal; 1: Asserted. (FAWS_TYPE_C)	0
			7	Laser Temperature High Alarm	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
			6	Laser Temperature High Warning	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
			5	Laser Temperature Low Warning	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
			4	Laser Temperature Low Alarm	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
			3	RX Power High Alarm	0: Normal; 1: Asserted. (FAWS_TYPE_B) The thresholds for the RX Power High/Low Alarm/Warning are determined by the RX Power Monitor Alarm/Warning Threshold Select in B015h. This comment applies to bits 2~0 as well.	0
			2	RX Power High Warning	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
			1	RX Power Low Warning	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
			0	RX Power Low Alarm	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0

Figure 55. CFP MSA Network Lane n Alarm and Warning 1

Network Lane VR 1						
Hex Addr	*Size*	*Access Type*	*Bit*	*Register Name* *Bit Field Name*	*Description*	*Init Value*
B190 [2.0]	**16**	**RO**		**Network Lane n Alarm and Warning 2**	**16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent.**	**0000h**
			15	Rx Laser Bias Current High Alarm	0: Normal, 1: Asserted (FAWS_TYPE_B)	0
			14	Rx Laser Bias Current High Warning	0: Normal, 1: Asserted (FAWS_TYPE_B)	0
			13	Rx Laser Bias Current Low Warning	0: Normal, 1: Asserted (FAWS_TYPE_B)	0
			12	Rx Laser Bias Current Low Alarm	0: Normal, 1: Asserted (FAWS_TYPE_B)	0
			11	Rx Laser Output High Alarm	0: Normal, 1: Asserted (FAWS_TYPE_B)	0
			10	Rx Laser Output High Warning	0: Normal, 1: Asserted (FAWS_TYPE_B)	0
			9	Rx Laser Output Low Warning	0: Normal, 1: Asserted (FAWS_TYPE_B)	0
			8	Rx Laser Output Low Alarm	0: Normal, 1: Asserted (FAWS_TYPE_B)	0
			7	Rx Laser Temp High Alarm	0: Normal, 1: Asserted (FAWS_TYPE_B)	0
			6	Rx Laser Temp High Warning	0: Normal, 1: Asserted (FAWS_TYPE_B)	0
			5	Rx Laser Temp Low Warning	0: Normal, 1: Asserted (FAWS_TYPE_B)	0
			4	Rx Laser Temp Low Alarm	0: Normal, 1: Asserted (FAWS_TYPE_B)	0
			3	Tx Modulator Bias High Alarm	0: Normal, 1: Asserted (FAWS_TYPE_B)	0
			2	Tx Modulator Bias High Warning	0: Normal, 1: Asserted (FAWS_TYPE_B)	0
			1	Tx Modulator Bias Low Warning	0: Normal, 1: Asserted (FAWS_TYPE_B)	0
			0	Tx Modulator Bias Low Alarm	0: Normal, 1: Asserted (FAWS_TYPE_B)	0

Figure 56. CFP MSA Network Lane n Alarm and Warning 2

- **Latch:**

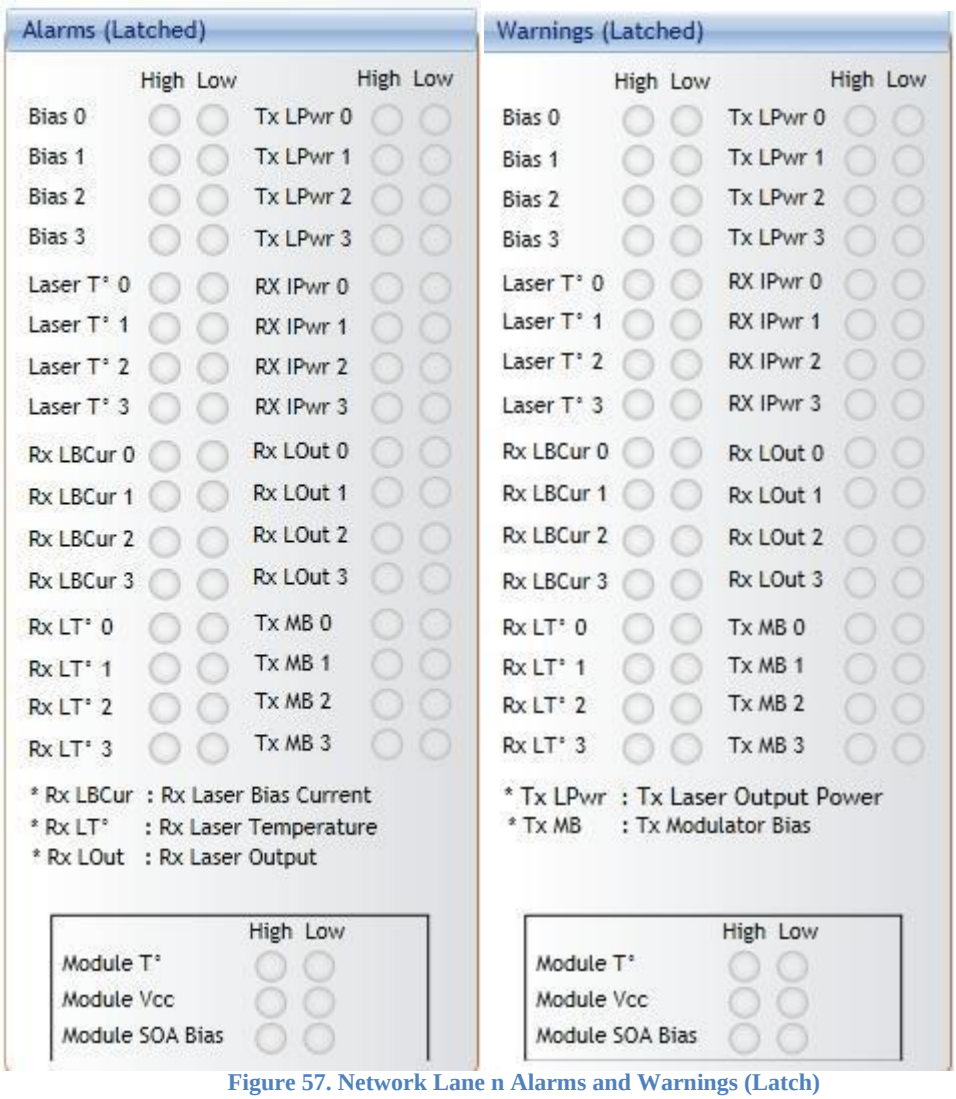


Figure 57. Network Lane n Alarms and Warnings (Latch)

B1B0 [2.0]	16	RO/LH/ COR		Network Lane n Alarm and Warning 1 Latch	16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent.	0000h
			15	Bias High Alarm Latch	1: Latched.	0
			14	Bias High Warning Latch	1: Latched.	0
			13	Bias Low Warning Latch	1: Latched.	0
			12	Bias Low Alarm Latch	1: Latched.	0
			11	TX Power High Alarm Latch	1: Latched.	0
			10	TX Power High Warning Latch	1: Latched.	0
			9	TX Power Low Warning Latch	1: Latched.	0
			8	TX Power Low Alarm Latch	1: Latched.	0
			7	Laser Temperature High Alarm Latch	1: Latched.	0
			6	Laser Temperature High Warning Latch	1: Latched.	0
			5	Laser Temperature Low Warning Latch	1: Latched.	0
			4	Laser Temperature Low Alarm Latch	1: Latched.	0
			3	RX Power High Alarm Latch	1: Latched. The thresholds for the RX Power High/Low Alarm/Warning are determined by the RX Power Monitor Alarm/Warning Threshold Select in B015h. This comment applies to bits 2~0 as well.	0
			2	RX Power High Warning Latch	1: Latched.	0
			1	RX Power Low Warning Latch	1: Latched.	0
			0	RX Power Low Alarm Latch	1: Latched.	0

Figure 58. CFP MSA Network Lane n Alarm and Warning 1 Latch

B1C0 [2.0]	16	RO/LH/ COR		Network Lane n Alarm and Warning 2 Latch	16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent.	0000h
			15	Rx Laser Bias High Alarm Latch	1: Latched	0
			14	Rx Laser Bias High Warning Latch	1: Latched	0
			13	Rx Laser Bias Low Warning Latch	1: Latched	0
			12	Rx Laser Bias Low Alarm Latch	1: Latched	0
			11	Rx Laser Output High Alarm Latch	1: Latched	0
			10	Rx Laser Output High Warning Latch	1: Latched	0
			9	Rx Laser Output Low Warning Latch	1: Latched	0
			8	Rx Laser Output Low Alarm Latch	1: Latched	0
			7	Rx Laser Temp High Alarm Latch	1: Latched	0
			6	Rx Laser Temp High Warning Latch	1: Latched	0
			5	Rx Laser Temp Low Warning Latch	1: Latched	0
			4	Rx Laser Temp Low Alarm Latch	1: Latched	0
			3	Tx Modulator Bias High Alarm Latch	1: Latched	0
			2	Tx Modulator Bias High Warning Latch	1: Latched	0
			1	Tx Modulator Bias Low Warning Latch	1: Latched	0
			0	Tx Modulator Bias Low Alarm Latch	1: Latched	0

Figure 59. CFP MSA Network Lane n Alarm and Warning 2 Latch

8.6.9.6 Measurements

The measurements are always shown whether we are reading the current or latch registers.

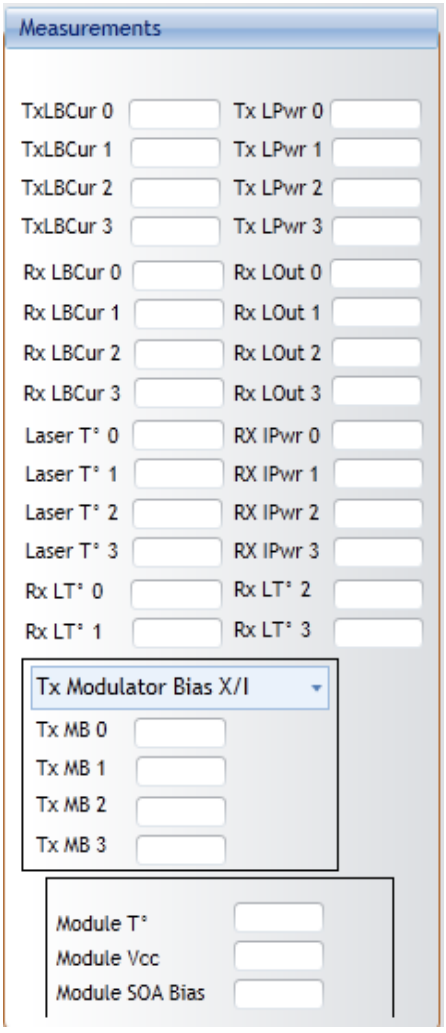


Figure 60. Measurements

				Network Lane A/D Value Measurement Registers		
B320 [2.0]	16	RO	15~0	Network Lane n TX Laser Bias Current monitor A/D value	16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent. Measured laser bias current in uA, a 16-bit unsigned integer with LSB = 2 uA, representing a total measurement range of 0 to 131.072 mA. Minimum accuracy shall be +/- 10% of the nominal value over temperature and voltage. This register is for CFP MSA modules.	0000h
B330 [2.0]	16	RO	15~0	Network Lane n TX Laser Output Power monitor A/D value	16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent. Measured TX laser output power in dBm, a signed 16-bit integer with LSB = 0.01 dBm. Accuracy must be better than +/- 2 dB over temperature and voltage range. Relative accuracy must be better than 1 dB.	0000h
B340 [2.0]	16	RO	15~0	Network Lane n TX Laser Temp Monitor A/D value	16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent. Internally measured temperature in degrees Celsius, a 16-bit signed integer with LSB = 1/256 of a degree Celsius, representing a total range from -128 to + 127 255/256 degC. MSA valid range is between –40 and +125C. Minimum accuracy is +/- 3 degC over temperature range.	0000h
B350 [2.0]	16	RO	15~0	Network Lane n RX Input Power monitor A/D value	16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent. Measured received input power in uW, a 16-bit unsigned integer with LSB = 0.1 uW, representing a power range from 0 to 6.5535 mW (-40 to +8.2 dBm). Value can represent either average received power or OMA depending upon how bit 3 of Register 8080h is set. Accuracy must be better than +/- 2dB over temperature and voltage. This accuracy shall be maintained for input power levels up to the lesser of maximum transmitted or maximum received optical power per the appropriate standard. It shall be maintained down to the minimum transmitted power minus cable plant loss per the appropriate standard. Relative accuracy shall be better than 1 dB over the received power range, temperature range, voltage range, and the life of the product.	0000h

B360 [2.0]	16	RO	15~0	Network Lane n TX Laser Bias Current monitor A/D value	16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent. TX laser bias current monitor in uA, an unsigned 16-bit integer with LSB = 100uA, representing a total measurement range of 0 to 6553.5 mA. Minimum accuracy is +/- 10% of the nominal value over temperature and voltage.	0000h
B370 [2.0]	16	RO	15~0	Network Lane n RX Laser Bias Current monitor A/D values.	16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent. Measured RX laser bias current in uA, an unsigned 16-bit integer with LSB = 100 uA, representing a total measurement range of 0 to 6553.5 mA. Minimum accuracy is +/- 10% of the nominal value over temperature and voltage.	0000h
B380 [2.0]	16	RO	15~0	Network Lane n RX Laser Temp Monitor A/D value.	16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent. Internally measured temperature in degrees Celsius, a signed 16-bit integer with LSB = 1/256 of a degree Celsius, representing a total range from -128 to + 127 255/256 degC. MSA valid range is between –40 and +125C. Minimum accuracy is +/- 3 degC over t	0000h
B390 [2.0]	16	RO	15~0	Network Lane n RX Laser Output Power Monitor A/D value	16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent. Measured RX laser output power in dBm, a signed 16-bit integer with the LSB = 0.01 dBm	0000h
B3A0 [2.0]	16	RO	15~0	TX Modulator Bias X/I Monitor A/D value	16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent. TX Modulator Bias, a 16-bit unsigned integer with LSB = 2mV, yielding a total measurement range of 0 to 131.072 Volts. Accuracy shall be better than +/-3% of the nominal value over specified operating temperature and voltage range.	0
B3B0 [2.0]	16	RO	15~0	TX Modulator Bias X/Q Monitor A/D value		0
B3C0 [2.0]	16	RO	15~0	TX Modulator Bias Y/I Monitor A/D value		0
B3D0 [2.0]	16	RO	15~0	TX Modulator Bias Y/Q Monitor A/D value		0
B3E0 [2.0]	16	RO	15~0	TX Modulator Bias X_Phase Monitor A/D value		0
B3F0 [2.0]	16	RO	15~0	TX Modulator Bias Y_Phase Monitor A/D value		0

Figure 61. CFP MSA Network Lane A/D Value Measurement Registers

B030 [2.0]	1	RO	15~0	Module Power Supply Monitor A/D Value	Internally measured transceiver supply voltage, a 16-bit unsigned integer with LSB = 1 mV, yielding a total measurement range of 0 to 65.535 V. Accuracy shall be better than +/- 3% of the nominal value over specified temperature and voltage ranges.	0000h
B031 [2.0]	1	RO	15~0	SOA Bias Current A/D Value	Measured SOA bias current in uA, a 16-bit unsigned integer with LSB = 2 uA, representing a total range of from 0 to 131.072 mA. Accuracy shall be better than +/- 10% of the nominal value over specified temperature and voltage.	0000h
B02F [2.0]	1	RO	15~0	Module Temp Monitor A/D Value	Internally measured temperature in degrees Celsius, a 16-bit signed integer with LSB = 1/256 of a degree Celsius, representing a total range from -128 to + 127 255/256 degC. MSA valid range is between –40 and +125C. Accuracy shall be better than +/- 3 degC over the whole temperature range.	0000h

Figure 62. CFP MSA Module Analog A/D Value Registers

8.6.10 Interrupt Masks ACO

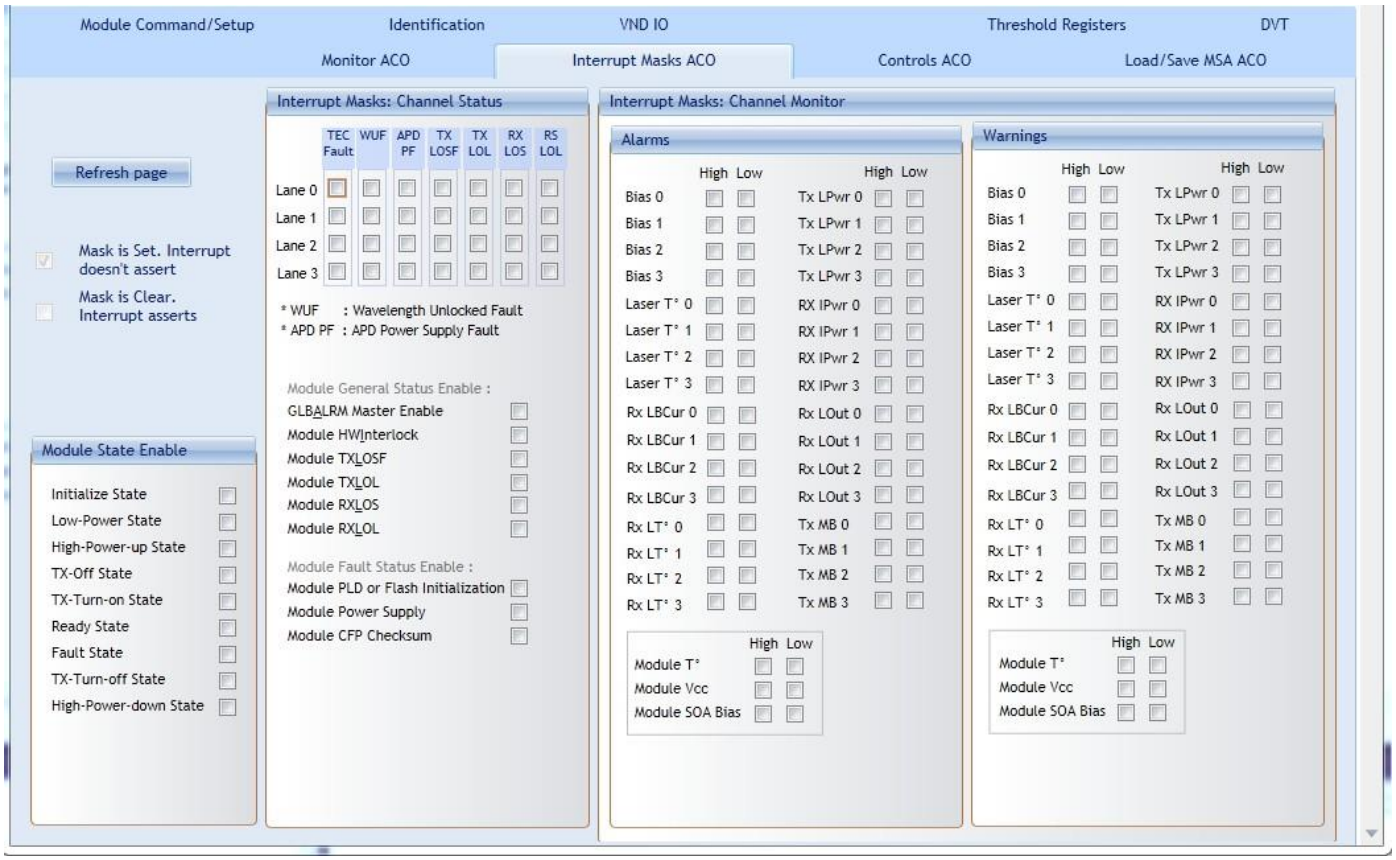


Figure 63. Interrupt Masks ACO tab

8.6.10.1 Module State Enable

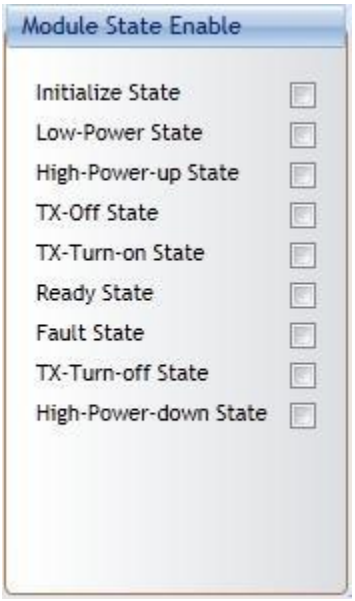


Figure 64. Module State Enable

Module FAWS Enable Registers						
B028 [2.0]	**1**			**Module State Enable**	**GLB_ALRM Enable register for Module State change. One bit for each state.**	**006Ah**
		RO	15~9	Reserved		0
		RW	8	High-Power-down State Enable	1: Enable corresponding signal to assert GLB_ALRM.	0
		RW	7	TX-Turn-off State Enable	1: Enable corresponding signal to assert GLB_ALRM.	0
		RW	6	Fault State Enable	1: Enable corresponding signal to assert GLB_ALRM. (Init Value is 1 to allow GLB_ALRM in startup sequence.)	1
		RW	5	Ready State Enable	1: Enable corresponding signal to assert GLB_ALRM. (Init Value is 1 to allow GLB_ALRM in startup sequence.)	1
		RW	4	TX-Turn-on State Enable	1: Enable corresponding signal to assert GLB_ALRM.	0
		RW	3	TX-Off State Enable	1: Enable corresponding signal to assert GLB_ALRM. (Init Value is 1 to allow GLB_ALRM in startup sequence.)	1
		RW	2	High-Power-up State Enable	1: Enable corresponding signal to assert GLB_ALRM.	0
		RW	1	Low-Power State Enable	1: Enable corresponding signal to assert GLB_ALRM. (Init Value is 1 to allow GLB_ALRM in startup sequence)	1
		RO	0	Initialize State Enable	1: Enable corresponding signal to assert GLB_ALRM.	0

Figure 65. CFP MSA Module FAWS Enable Registers

8.6.10.2 Interrupt Masks: Channel Status

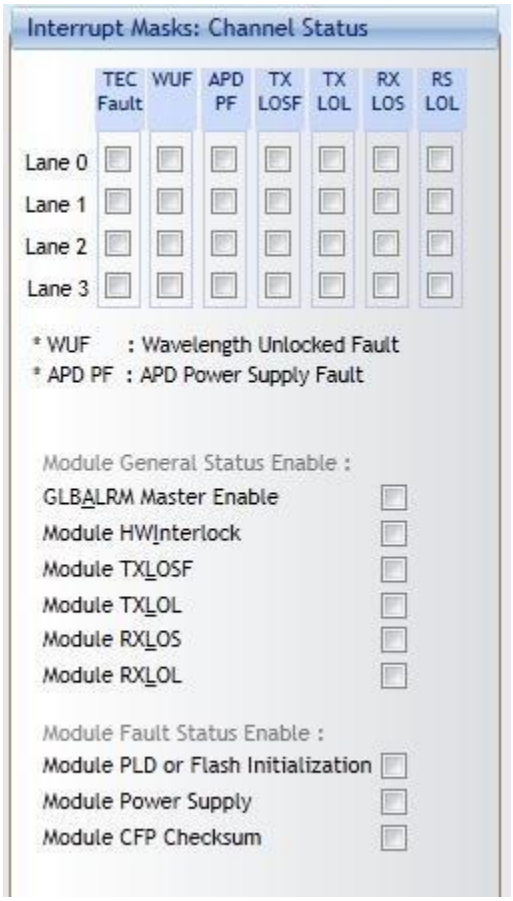


Figure 66. Interrupt Masks: Channel Status

B200 [2.0]	**16**			**Network Lane n Fault and Status Enable**	**16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent.**	**E0D Ch**
		RW	15	Lane TEC Fault Enable	0: Disable, 1: Enable.	1
		RW	14	Lane Wavelength Unlocked Fault Enable	0: Disable, 1: Enable.	1
		RW	13	Lane APD Power Supply Fault Enable	0: Disable, 1: Enable.	1
		RO	12~8	Reserved		0
		RW	7	Lane TX_LOSF Enable	0: Disable, 1: Enable.	1
		RW	6	Lane TX_LOL Enable	0: Disable, 1: Enable.	1
		RO	5	Reserved		0
		RW	4	Lane RX_LOS Enable	0: Disable, 1: Enable.	1
		RW	3	Lane RX_LOL Enable	0: Disable, 1: Enable.	1
		RW	2	Lane RX FIFO Status Enable	0: Disable, 1: Enable.	1
		RW	1	Lane RX TEC Fault Enable	0: Disable, 1: Enable.	1
		RO	0	Reserved		0

Figure 67. CFP MSA Network Lane n Fault and Status Enable

B029 [2.0]	**1**			**Module General Status Enable**	**1: Enable signal to assert GLB_ALRM. Bits 14~0 are AND'ed with corresponding bits in the Module General Status Latch register; the result is used to assert GLB_ALRM. Bit 15 is the master enable of GLB_ALRM and it is AND'ed with the output of the "OR" gate output in Global Alarm Signal Aggregation, Figure 10.**	**A7F8h**
		RW	15	GLB_ALRM Master Enable	1: Enable.	1
		RO	14	Reserved		0
		RW	13	HW_Interlock	1: Enable. For non-pluggable modules (e.g. MSA-100GLH module), this bit is not read.	1
		RO	12~11	Reserved		0
		RW	10	Loss of REFCLK Input Enable	1: Enable.	1
		RW	9	TX_JITTER_PLL_LOL Enable	1: Enable.	1
		RW	8	TX_CMU_LOL Enable	1: Enable.	1
		RW	7	TX_LOSF Enable	1: Enable.	1
		RW	6	TX_HOST_LOL Enable	1: Enable.	1
		RW	5	RX_LOS Enable	1: Enable.	1
		RW	4	RX_NETWORK_LOL Enable	1: Enable.	1
		RW	3	Out of Alignment Enable	1. Enable.	1
		RW	2	Performance Monitor Interval Complete Enable	1. Enable.	1
		RO	1~0	Reserved		000b

Figure 68. CFP MSA Module General Status Enable

B02A [2.0]	**1**			**Module Fault Status Enable**	**These bits are AND'ed with corresponding bits in the Module Fault Latch register; the result is used to assert GLB_ALRM. Optional features that are not implemented shall have their Enable bit forced to '0'.**	**0062h**
		RO	15~7	Reserved		0
		RW	6	PLD or Flash Initialization Fault Enable	1: Enable.	1
		RW	5	Power Supply Fault Enable	1: Enable.	1
		RO	4~2	Reserved		000b
		RW	1	CFP Checksum Fault Enable	1: Enable.	1
		RO	0	Reserved		0

Figure 69. CPF MSA Module Fault Status Enable

8.6.10.3 Interrupt Masks: Channel Monitor-Alarms and Warnings

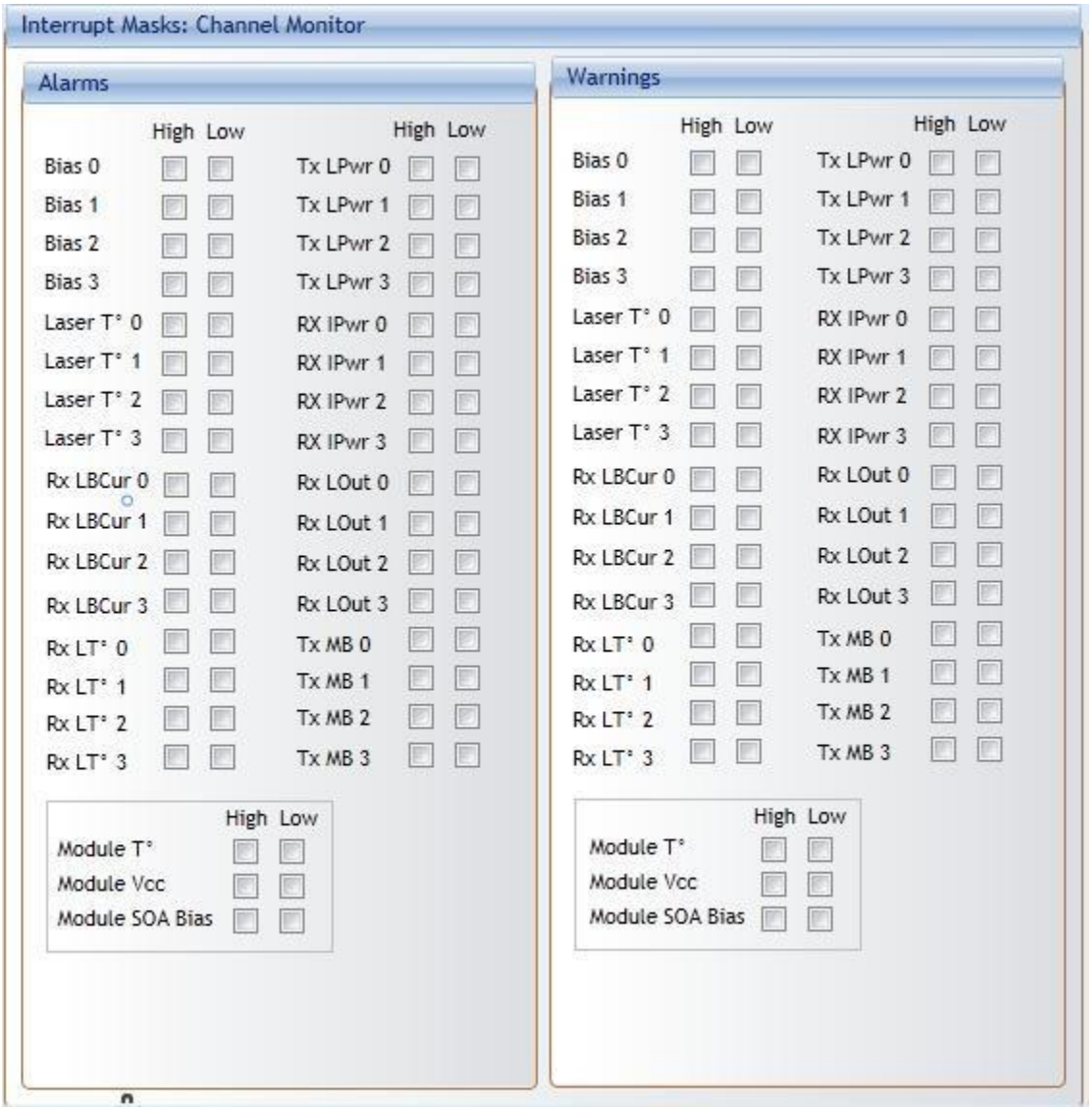


Figure 70. Interrupt Masks: Channel Monitor

Network Lane FAWS Enable Registers						
B1E0 [2.0]	**16**	**RW**		**Network Lane n Alarm and Warning 1 Enable**	**16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent.**	**FFFF h**
			15	Bias High Alarm Enable	0: Disable, 1: Enable.	1
			14	Bias High Warning Enable	0: Disable, 1: Enable.	1
			13	Bias Low Warning Enable	0: Disable, 1: Enable.	1
			12	Bias Low Alarm Enable	0: Disable, 1: Enable.	1
			11	TX Power High Alarm Enable	0: Disable, 1: Enable.	1
			10	TX Power High Warning Enable	0: Disable, 1: Enable.	1
			9	TX Power Low Warning Enable	0: Disable, 1: Enable.	1
			8	TX Power Low Alarm Enable	0: Disable, 1: Enable.	1
			7	Laser Temperature High Alarm Enable	0: Disable, 1: Enable.	1
			6	Laser Temperature High Warning Enable	0: Disable, 1: Enable.	1
			5	Laser Temperature Low Warning Enable	0: Disable, 1: Enable.	1
			4	Laser Temperature Low Alarm Enable	0: Disable, 1: Enable.	1
			3	RX Power High Alarm Enable	0: Disable, 1: Enable This comment applies to bits 2~0 as well.. The thresholds for the RX Power High/Low Alarm/Warning are determined by the RX Power Monitor Alarm/Warning Threshold Select in B015h.	1
			2	RX Power High Warning Enable	0: Disable, 1: Enable.	1
			1	RX Power Low Warning Enable	0: Disable, 1: Enable.	1
			0	RX Power Low Alarm Enable	0: Disable, 1: Enable.	1
B1F0 [2.0]	**16**	**RW**		**Network Lane n Alarm and Warning 2 Enable**	**16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent.**	**FFFF h**
			15	Rx Laser Bias Current High Alarm Enable	0: Disable, 1: Enable.	1
			14	Rx Laser Bias Current High Warning Enable	0: Disable, 1: Enable.	1
			13	Rx Laser Bias Current Low Warning Enable	0: Disable, 1: Enable.	1
			12	Rx Laser Bias Current Low Alarm Enable	0: Disable, 1: Enable.	1
			11	Rx Laser Output High Alarm Enable	0: Disable, 1: Enable.	1
			10	Rx Laser Output High Warning Enable	0: Disable, 1: Enable.	1
			9	Rx Laser Output Low Warning Enable	0: Disable, 1: Enable.	1
			8	Rx Laser Output Low Alarm Enable	0: Disable, 1: Enable.	1
			7	Rx Laser Temp High Alarm Enable	0: Disable, 1: Enable.	1
			6	Rx Laser Temp High Warning Enable	0: Disable, 1: Enable.	1
			5	Rx Laser Temp Low Warning Enable	0: Disable, 1: Enable.	1
			4	Rx Laser Temp Low Alarm Enable	0: Disable, 1: Enable.	1
			3	Tx Modulator Bias High Alarm Enable	0: Disable, 1: Enable.	1
			2	Tx Modulator Bias High Warning Enable	0: Disable, 1: Enable.	1
			1	Tx Modulator Bias Low Warning Enable	0: Disable, 1: Enable.	1
			0	Tx Modulator Bias Low Alarm Enable	0: Disable, 1: Enable.	1

Figure 71. CFP MSA Network FAWS Enable Registers

B02B [2.0]	**1**			**Module Alarm and Warning 1 Enable**	**These bits are AND'ed with corresponding bits in the Module Alarm and Warning 1 Latch register; the result is used to assert GLB_ALRM. Optional features that are not implemented shall have their Enable bit forced to '0'.**	**0FFFh**
		RO	15~12	Reserved		0000b
		RW	11	Mod Temp Hi Alarm Enable	1: Enable.	1
			10	Mod Temp Hi Warn Enable	1: Enable.	1
			9	Mod Temp Low Warning Enable	1: Enable.	1
			8	Mod Temp Low Alarm Enable	1: Enable.	1
			7	Mod Vcc High Alarm Enable	1: Enable.	1
			6	Mod Vcc High Warning Enable	1: Enable.	1
			5	Mod Vcc Low Warning Enable	1: Enable.	1
			4	Mod Vcc Low Alarm Enable	1: Enable.	1
			3	Mod SOA Bias High Alarm Enable	1: Enable.	1
			2	Mod SOA Bias High Warning Enable	1: Enable.	1
			1	Mod SOA Bias Low Warning Enable	1: Enable.	1
			0	Mod SOA Bias Low Alarm Enable	1: Enable.	1

Figure 72. CFP MSA Module Alarm and Warning 1 Enable

8.6.11 Controls ACO

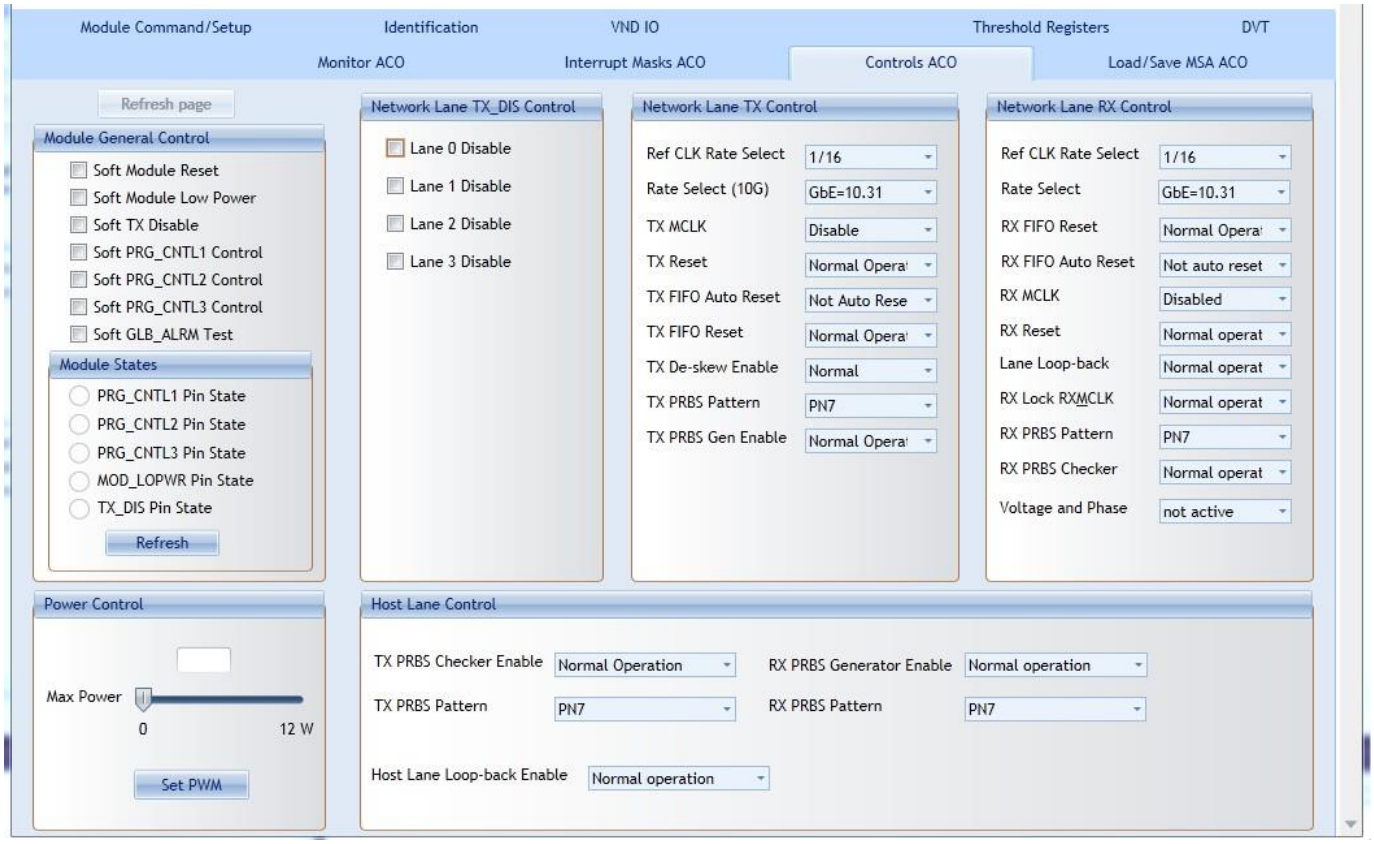


Figure 73. Controls ACO tab

8.6.11.1 Module General Control And States

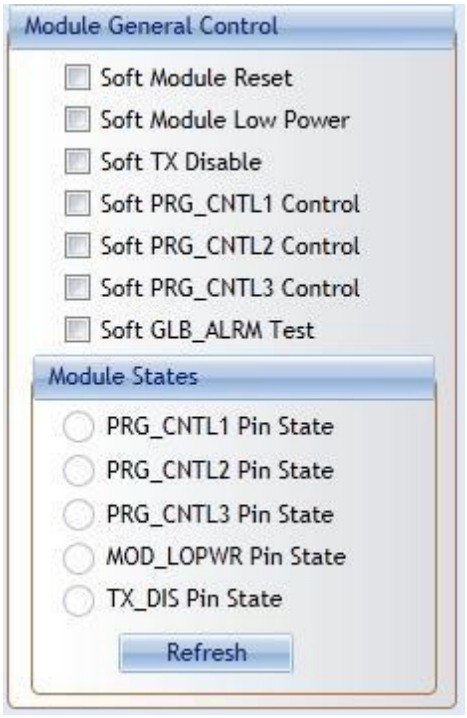


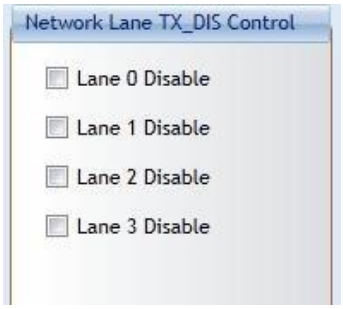
Figure 74. Module General Control and States

Module Control Registers						
B010 [2.0]	**1**			**Module General Control**		**0000h**
		RW/SC/LH	15	Soft Module Reset	Register bit for module reset function. Writing a 0 to this bit has no effect regardless it was 0 or 1 previously. 1: Module reset assert.	0
		RW	14	Soft Module Low Power	Register bit for module low power function. 1: Assert.	0
		RW	13	Soft TX Disable	Register bit for TX Disable function. 1: Assert.	0
		RW	12	Soft PRG_CNTL3 Control	Register bit for PRG_CNTL3 control function. 1: Assert.	0
		RW	11	Soft PRG_CNTL2 Control	Register bit for PRG_CNTL2 control function. 1: Assert.	0
		RW	10	Soft PRG_CNTL1 Control	Register bit for PRG_CNTL1 control function. 1: Assert.	0
		RW	9	Soft GLB_ALRM Test	Command bit for software forced test signal. When this bit is asserted it generates GLB_ALRM signal. 1: Assert.	0
		RW/SC	8	Processor Reset	Register bit for processor reset function. This bit is self-clearing. Register settings are not affected. This is a Non-Service Affecting reset. 1: Assert.	0
		RO	7~6	Reserved		0
		RO	5	TX_DIS Pin State	Logical state of the TX_DIS pin. 1: Assert.	0
		RO	4	MOD_LOPWR Pin State	Logical state of the MOD_LOPWR pin. 1: Assert.	0
		RO	3	PRG_CNTL3 Pin State	Logical state of the PRG_CNTL3 pin.	0

					1: Assert.	
		RO	2	PRG_CNTL2 Pin State	Logical state of the PRG_CNTL2 pin. 1: Assert.	0
		RO	1	PRG_CNTL1 Pin State	Logical state of the PRG_CNTL1 pin. 1: Assert.	0
		RO	0	Reserved		0

Figure 75. CFP MSA Module Control Registers

8.6.11.2 Network Lane TX_DIS Control



B013 [2.0]	**1**	**RW**		**Individual Network Lane TX_DIS Control**	**This register acts upon individual network lanes. Note that toggling individual network lane TX disable bit does not change module state.**	**0000h**
			15~0	Lane n Disable	Bits 15~0 disable Lanes 15~0 respectively. 0: Normal, 1: Disable.	0

Figure 76. CFP MSA Individual Network Lane TX_DIS Control

8.6.11.3 Network Lane TX Control

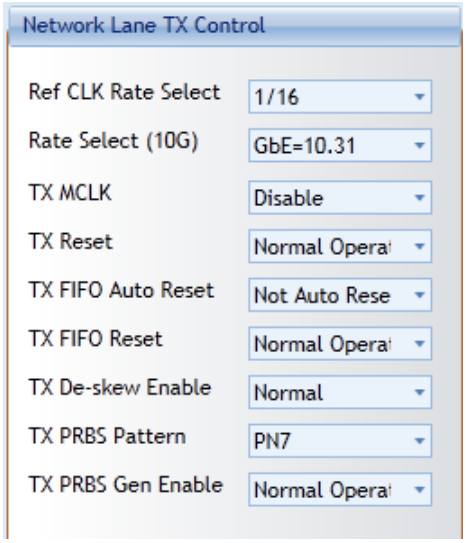


Figure 77. Network Lane TX Control

B011 [2.0]	**1**			**Network Lane TX Control**	**This control acts upon all the network lanes.**	**0200h**
		RO	15	Reserved		0
		RW	14	TX PRBS Generator Enable	0: Normal operation, 1: PRBS mode. (Optional)	0
		RW	13~12	TX PRBS Pattern	00b:2^7, 01b:2^15, 10b:2^23, 11b:2^31.	00b
		RW	11	TX De-skew Enable	0:Normal, 1:Disable	0
		RW	10	TX FIFO Reset	This bit affects both host and network side TX FIFOs. 0: Normal operation, 1: Reset (Optional).	0
		RW	9	TX FIFO Auto Reset	This bit affects both host and network side TX FIFOs. 0: Not Auto Reset, 1: Auto Reset. (Optional).	1
		RW	8	TX Reset	0: Normal operation, 1: Reset. Definition and implementation are vendor specific.	0
		RW [2.2]	7~5	TX MCLK Control	3-bit field coding the MCLK rate control.	000b
					Code / **Description** / **CFP** / **CFP2/4**	
					000b / Function disabled	
					001b / Of network lane rate / Reserved / 1/32	
					010b / Of network lane rate / 1/8 / 1/8	
					011b / Of host lane rate / Reserved / Reserved	
					100b / Of network lane rate / 1/64 / Reserved	
					101b / Of host lane rate / 1/64 / 1/160	
					110b / Of network lane rate / 1/16 / Reserved	
					111b / Of host lane rate / 1/16 / 1/40	
		RO	4	Reserved		0b
		RW	3~1	TX Rate Select (10G lane rate)	000b: GbE=10.31, 001b: SDH=9.95, 010b: OTU3=10.7, 011b: OTU4=11.2, 100b: OTU3e1=11.14, 101b: OTU3e2=11.15, 110b~111b: Reserved.	000b
		RW	0	TX Reference CLK Rate Select	0: 1/16, 1: 1/64.	0b

Figure 78. CFP MSA Netwok Lane TX Control

8.6.11.4 *Network Lane RX Control*

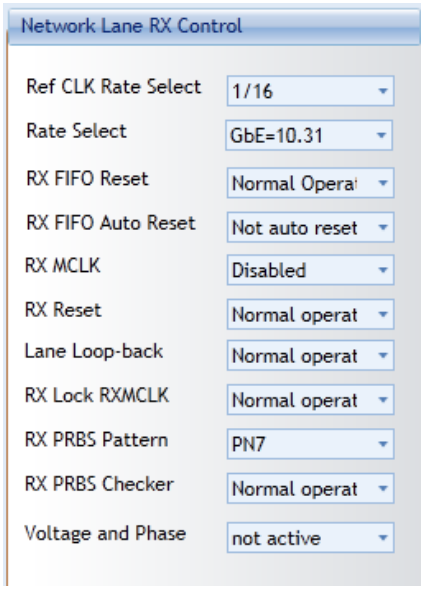


Figure 79. Network Lane RX Control

B012 [2.0]	**1**			**Network Lane RX Control**	**This control acts upon all the network lanes.**	**0200h**
		RW	15	Active Decision Voltage and Phase function	This bit activates the active decision voltage and phase function in the module. 0: not active, 1: active. (Optional)	0b
		RW	14	RX PRBS Checker Enable	0: Normal operation, 1: PRBS mode. (Optional)	0b
		RW	13~12	RX PRBS Pattern	00b: 2^7, 01b: 2^15, 10b: 2^23, 11b: 2^31.	00b
		RW	11	RX Lock RX_MCLK to Reference CLK	0: Normal operation, 1: Lock RX_MCLK to REFCLK.	0b
		RW	10	Network Lane Loop-back	0: Normal operation, 1: Network lane loop-back. (Optional)	0b
		RW	9	RX FIFO Auto Reset	0: Not auto reset, 1: Auto reset. (Optional).	1b
		RW	8	RX Reset	0: Normal operation, 1: Reset. Definition and implementation are vendor specific.	0b
		RW [2.2]	7~5	RX MCLK Control (optional)	3-bit field coding the MCLK rate control.	000b
					Code / Description / CFP / CFP2/4	
					000b / Function disabled	
					001b / Of network lane rate / Reserved / 1/32	
					010b / Of network lane rate / 1/8 / 1/8	
					011b / Of host lane rate / Reserved / Reserved	
					100b / Of network lane rate / 1/64 / Reserved	
					101b / Of host lane rate / 1/64 / 1/160	
					110b / Of network lane rate / 1/16 / Reserved	
					111b / Of host lane rate / 1/16 / 1/40	
		RW	4	RX FIFO Reset	0: Normal, 1: Reset. (Optional).	0b
		RW	3~1	RX Rate Select	000b: GbE=10.31, 001b:SDH=9.95, 010b:OTU3=10.7, 011b:OTU4=11.2, 100b:OTU3e1=11.14, 101b OTU3e2=11.15, 110b~111b: Reserved.	000b
		RW	0	RX Reference CLK Rate Select	0: 1/16, 1: 1/64.	1b

Figure 80. CFP MSA Network Lane RX Control Registers

8.6.11.5 Power Control

Figure 81. Power Control

The user can specify the maximum power consumed by the CFP2 module. He should adjust Max Power to the desired value, then press Set PWM to set the maximum allowed values for each thermal spot.

8.6.11.6 Host Lane Control

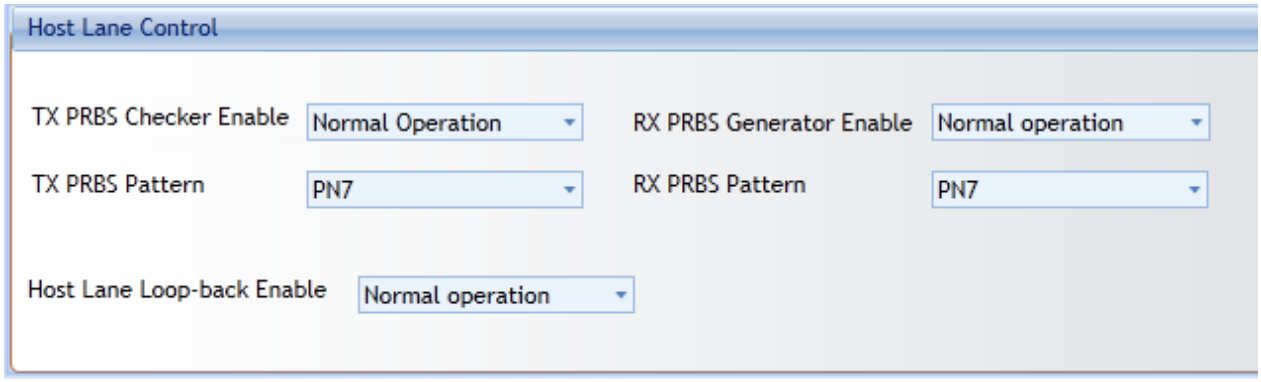


Figure 82. Host Lane Control

B014 [2.0]	**1**			**Host Lane Control**	**This control acts upon all the host lanes.**	**0000h**
		RO	15	Reserved		0
		RW	14	TX PRBS Checker Enable	0: Normal operation, 1: PRBS mode. (Optional)	0
		RW	13	TX PRBS Pattern 1	00:2^7, 01:2^15, 10:2^23, 11:2^31.	00b
		RW	12	TX PRBS Pattern 0		
		RO	11	Reserved		0
		RW	10	Host Lane Loop-back Enable	0: Normal operation, 1: Host lane loop-back. (Optional)	0
		RO	9			0
		RO	8	Reserved		0
		RW	7	RX PRBS Generator Enable	0: Normal operation, 1: PRBS mode. (Optional)	0
		RW	6	RX PRBS Pattern 1	00b: 2^7, 01b: 2^15, 10b: 2^23, 11b: 2^31.	00b
		RW	5	RX PRBS Pattern 0		
		RO	4~0	Reserved		0h

Figure 83. CFP MSA Host Lane Control

8.6.12 Load/Save MSA ACO

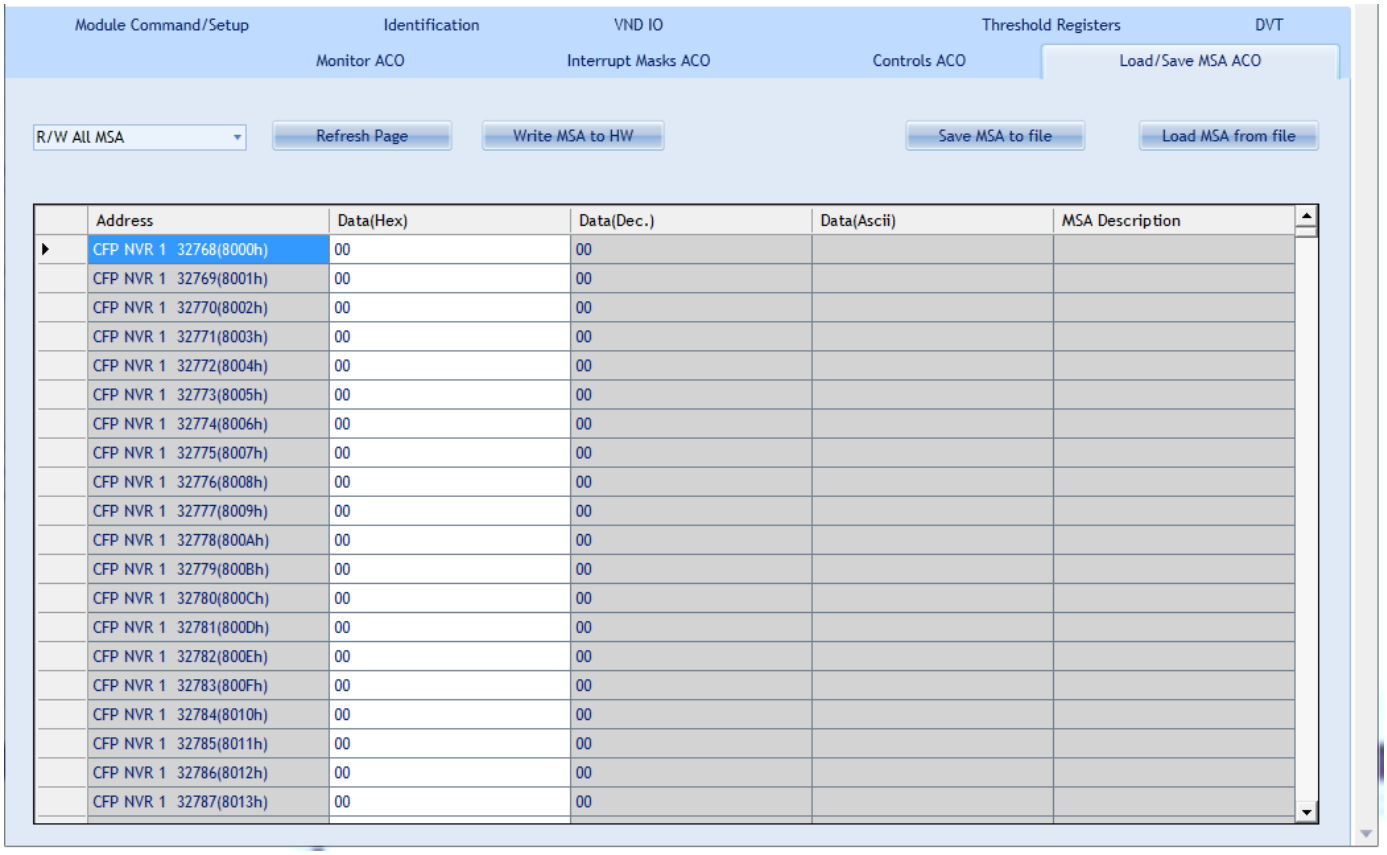


Figure 84. Load/Save MSA ACO tab

This screen allows user to Load or Save his custom CFP2 ACO configuration.
Once data is gathered, it will be displayed in a grid showing: register address, hex value, ASCII value, register description.

- **Refresh Page button:** Read CFP MSA Registers, and refresh values.
- **Write MSA to HW button:** Write the current MSA configuration to CFP2 module.
- **Save MSA to file button:** saves the current MSA memory to a file using CSV (comma separated values) format.
- **Load MSA from file button:** Loads MSA values from file and map it to MSA memory.

Note that the user can choose from the drop down list whether to read/write:

- ✓ Volatile registers
- ✓ Non volatile registers
- ✓ All MSA registers without

P.S: These registers exclude the reserved addresses.

Additional Control

8.6.13 Changing Port Address

When the module is initialized, the default port address is automatically set to 0.

However the user will be able to change the Port Address anytime by entering the new Hexadecimal value in the textbox shown in the below Figure and Press the Set button.

Figure 85 GUI Header

8.6.14 Additional GUI tabs

Two tabs can be brought up to allow additional control:

1- Threshold registers tab

2- DVT tab

In order to show these tabs, user can double click on the CFP2 Host label that is shown on Figure 43 above, the following Maintenance window will show up:

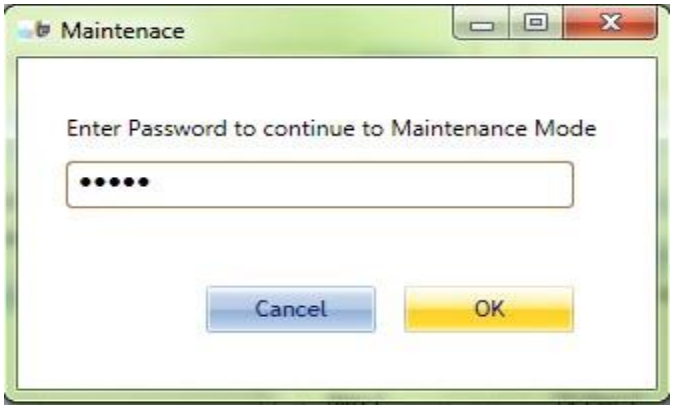


Figure 86 Maintenance window

The password to be entered is: MLCFP

When you press the OK button you will recognize that 2 new tabs are now available on the GUI, as the below figure shows:

Figure 87 Additional tabs

8.6.14.1 Threshold Registers

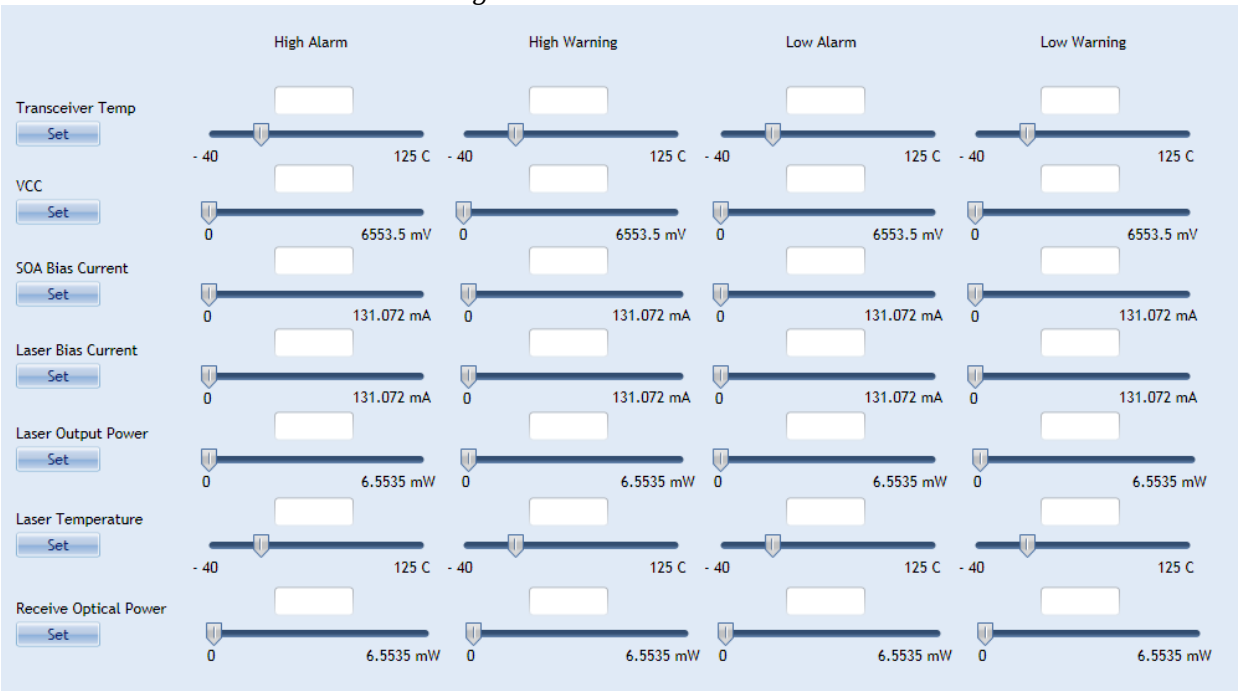


Figure 88. Threshold registers

This tab allows the user to update the values of the alarm and warning threshold registers.

the minimum and maximum scope of the values is as specified by CFP MSA.

Each A/D value has a corresponding high alarm, low alarm, high warning and low warning threshold.

The figure below shows the MSA memory map for the above values.

CFP NVR 2						
Hex Addr	***Size***	***Access Type***	***Bit***	***Register Name*** *Bit Field Name*	***Description***	***LSB Unit***
Alarm/Warning Threshold Registers						
8080	**2**	**RO**	**7~0**	**Transceiver Temp High Alarm Threshold**	**These thresholds are a signed 16-bit integer with LSB = 1/256 of a degree Celsius representing a range from -128 to + 127 255/256 degree C. MSA valid range is between –40 and +125C." MSB stored at low address, LSB stored at high address.**	**1/256 degC**
8082	**2**	**RO**	**7~0**	**Transceiver Temp High Warning Threshold**		
8084	**2**	**RO**	**7~0**	**Transceiver Temp Low Warning Threshold**		
8086	**2**	**RO**	**7~0**	**Transceiver Temp Low Alarm Threshold**		
8088	**2**	**RO**	**7~0**	**VCC High Alarm Threshold**	**These thresholds are an unsigned 16-bit integer with LSB = 0.1 mV, representing a range of voltage from 0 to 6.5535 V. MSB stored at low address, LSB stored at high address.**	**0.1 mV**
808A	**2**	**RO**	**7~0**	**VCC High Warning Threshold**		
808C	**2**	**RO**	**7~0**	**VCC Low Warning Threshold**		
808E	**2**	**RO**	**7~0**	**VCC Low Alarm Threshold**		
8090	**2**	**RO**	**7~0**	**SOA Bias Current High Alarm Threshold**	**These threshold values are an unsigned 16-bit integer with LSB = 2 uA, representing a range of current from 0 to 131.072 mA. MSB stored at low address, LSB stored at high address.**	**2 uA**
8092	**2**	**RO**	**7~0**	**SOA Bias Current High Warning Threshold**		
8094	**2**	**RO**	**7~0**	**SOA Bias Current Low Warning Threshold**		
8096	**2**	**RO**	**7~0**	**SOA Bias Current Low Alarm Threshold**		

8098	2	RO	7~0	Auxiliary 1 Monitor High Alarm Threshold	TBD	TBD
809A	2	RO	7~0	Auxiliary 1 Monitor High Warning Threshold	TBD	
809C	2	RO	7~0	Auxiliary 1 Monitor Low Warning Threshold	TBD	
809E	2	RO	7~0	Auxiliary 1 Monitor Low Alarm Threshold	TBD	
80A0	2	RO	7~0	Auxiliary 2 Monitor High Alarm Threshold	TBD	TBD
80A2	2	RO	7~0	Auxiliary 2 Monitor High Warning Threshold	TBD	
80A4	2	RO	7~0	Auxiliary 2 Monitor Low Warning Threshold	TBD	
80A6	2	RO	7~0	Auxiliary 2 Monitor Low Alarm Threshold	TBD	
80A8	2	RO	7~0	Laser Bias Current High Alarm Threshold	Alarm and warning thresholds for measured laser bias current. Reference A2A0h Description for additional information. MSB stored at low address, LSB stored at high address.	See A2A0h
80AA	2	RO	7~0	Laser Bias Current High Warning Threshold		
80AC	2	RO	7~0	Laser Bias Current Low Warning Threshold		
80AE	2	RO	7~0	Laser Bias Current Low Alarm Threshold		
80B0	2	RO	7~0	Laser Output Power High Alarm Threshold	Alarm and warning thresholds for measured laser output power. Reference A2B0h Description for additional information. MSB stored at	See A2B0h
80B2	2	RO	7~0	Laser Output Power High Warning Threshold		
80B4	2	RO	7~0	Laser Output Power Low Warning Threshold	low address, LSB stored at high address.	
80B6	2	RO	7~0	Laser Output Power Low Alarm Threshold		
80B8	2	RO	7~0	Laser Temperature High Alarm Threshold	Alarm and warning thresholds for measured received input power. Reference A2C0h Description for additional information. MSB stored at low address, LSB stored at high address.	See A2C0h
80BA	2	RO	7~0	Laser Temperature High Warning Threshold		
80BC	2	RO	7~0	Laser Temperature Low Warning Threshold		
80BE	2	RO	7~0	Laser Temperature Low Alarm Threshold		
80C0	2	RO	7~0	Receive Optical Power High Alarm Threshold	Alarm and warning thresholds for measured received input power. Reference A2D0h Description for additional information. MSB stored at low address, LSB stored at high address.	See A2D0h
80C2	2	RO	7~0	Receive Optical Power High Warning Threshold		
80C4	2	RO	7~0	Receive Optical Power Low Warning Threshold		
80C6	2	RO	7~0	Receive Optical Power Low Alarm Threshold		
80C8	55	RO	7~0	Reserved		0
80FF	1	RO	7~0	CFP NVR 2 Checksum	The 8-bit unsigned sum of all CFP NVR 2 contents from address 8080h through 80FEh inclusive.	NA

Figure 89. Threshold registers MSA memory map

8.6.14.2 DVT tab

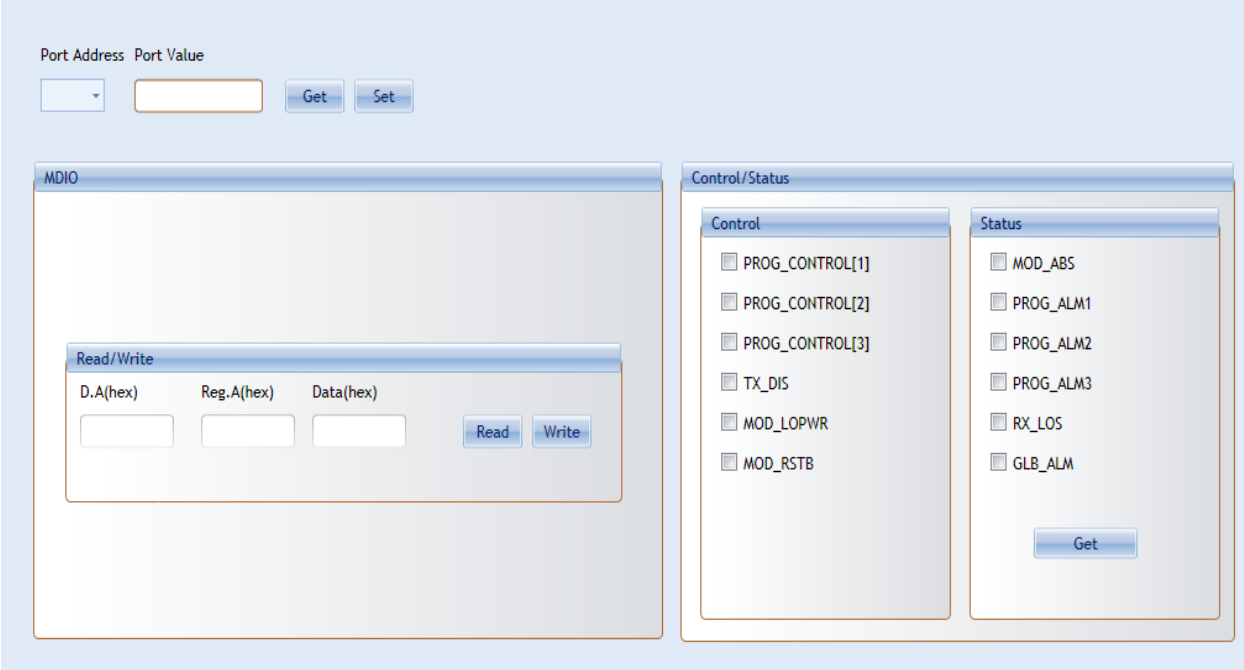


Figure 90. DVT tab

This tab allows user to directly control the ML4027/ML4042 Micro.

- One can choose a specific Port Address on the Micro and Get or Set its value(in Hex).
- Read/Write MDIO from a specific Device Address and Register Address.
- Change the control pins level.
- Get the Status pins values.

9. ML4028 CFP Break-Out

9.1 Product description

9.1.1 Overview

The ML4028 CFP2 Break-Out Module is designed to provide an efficient and easy method of interconnect testing between the host and a CFP2 module on a line card, blade or other type of PCB.
The ML4028 simply plugs into a MSA compliant CFP2 slot and provides high signal integrity characteristics. It comes complete with Huber & Suhner MXP connector rows.

9.1.2 Features

- Huber & Suhner MXP connectors.
- 1 coaxial pair for clock reference.
- High performance signal integrity traces from coax to interface.
- Operates at rate up to 28 Gb/s per channel.
- CFP2 MSA form factor.

9.1.3 Applications

- CFP2 line card testing
- System characterization.
- Signal integrity analysis of ASIC to CFP2 host connector.
- Receiver Tolerance testing of ASIC from CFP2 host connector.
- Functional verification using loopback functions.

9.2 Installing the CFP break out module

To install the CFP2 breakout module, follow these steps:
1. Attach an ESD wrist strap to yourself on one end and a properly grounded point on the chassis or the rack on the other end.
2. The CFP2 transceiver module is located inside its metallic shell.
3. Hold the shell so that the identifier label is on the top.
4. Align the CFP2 shell in front of the module's transceiver socket opening.
5. Carefully slide the CFP2 shell into the socket until the transceiver makes contact with the socket electrical connector.

10. ML4028-ACO CFP Break-Out

10.1 Product description

10.1.1 Overview

The ML4028-ACO CFP2 Break-Out Module is designed to provide an efficient and easy method of interconnect testing between the host and a CFP2 module on a line card, blade or other type of PCB.

The ML4028-ACO simply plugs into a MSA compliant CFP2 slot and provides high signal integrity characteristics. It comes complete with Huber & Suhner MXP connector rows.

10.1.2 Features

- 4 channels
- Huber & Suhner MXP connectors
- 1 coaxial pair for clock reference
- High performance signal integrity traces from coax to interface
- Operates at rate up to 28 Gb/s per channel
- CFP2 MSA form factor

10.1.3 Applications

- CFP2 line card testing
- System characterization
- Signal integrity analysis of ASIC to CFP2 host connector
- Receiver Tolerance testing of ASIC from CFP2 host connector
- Functional verification using loopback functions

10.2 Installing the CFP break out module

To install the CFP2 breakout module, follow these steps:

1. Attach an ESD wrist strap to yourself on one end and a properly grounded point on the chassis or the rack on the other end.
2. The CFP2 transceiver module is located inside its metallic shell.
3. Hold the shell so that the identifier label is on the top.
4. Align the CFP2 shell in front of the module's transceiver socket opening.
5. Carefully slide the CFP2 shell into the socket until the transceiver makes contact with the socket electrical connector.

11. Manual Revision History

This section describes the changes that were implemented in this document. The changes are listed by revision, starting with the most current publication.

Revision 0.0.1, December 12th, 2012: First Draft Release of this document.

Revision 0.0.2, March 18th, 2013: Modified Cut-Off Temperature register to 0x8402, and max PWM value to 102.

Revision 0.0.3, June 5th, 2013: corrected CFP2 BO name, corrected some paragraphs where ML4029 was referred to but it was written ML4028.

Revision 0.0.4, May 13th, 2014: Corrected register addresses in parag. 7.3.2, 7.1.6

Added section 7.3.3- RX_LOS (available in FW V3 for the ML4030)

Revision 0.0.6, Sept 11th, 2014: Added CFP2-ACO.